256-Position SPI-Compatible Digital Potentiometer

Data Sheet

AD5160

FEATURES

256-position
End-to-end resistance: 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ
Compact SOT-23-8 (2.9 mm × 3 mm) package
SPI-compatible interface
Power-on preset to midscale
Single supply: 2.7 V to 5.5 V
Low temperature coefficient: 45 ppm/°C
Low power, I_{DD} = 8 μA
Wide operating temperature: –40°C to +125°C
Evaluation board available

APPLICATIONS

Mechanical potentiometer replacement in new designs
Transducer adjustment of pressure, temperature, position, chemical, and optical sensors
RF amplifier biasing
Gain control and offset adjustment

FUNCTIONAL BLOCK DIAGRAM

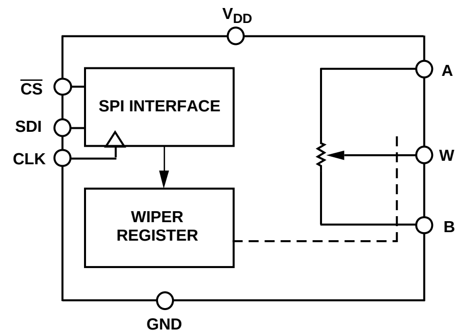

Figure 1.

PIN CONFIGURATION

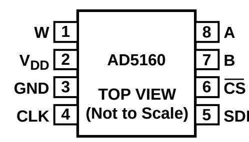

Figure 2.

GENERAL DESCRIPTION

The AD5160 provides a compact 2.9 mm × 3 mm packaged solution for 256-position adjustment applications. These devices perform the same electronic adjustment function as mechanical potentiometers[1] or variable resistors but with enhanced resolution, solid-state reliability, and superior low temperature coefficient performance.

The wiper settings are controllable through an SPI-compatible digital interface. The resistance between the wiper and either end point of the fixed resistor varies linearly with respect to the digital code transferred into the RDAC latch.

Operating from a 2.7 V to 5.5 V power supply and consuming less than 5 μA allows for usage in portable battery-operated applications.

[1] The terms digital potentiometer, VR, and RDAC are used interchangeably.

Rev. C Document Feedback

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REVISION HISTORY

11/14—Rev. B to Rev. C

Changes to Ordering Guide ... 16

5/09—Rev. A to Rev. B

Changes to Ordering Guide ... 16

1/09—Rev. 0 to Rev. A

Deleted Shutdown Supply Current Parameter and Endnote 7, Table 1 ... 3
Changes to Resistor Noise Voltage Density Parameter, Table 1 ... 3
Deleted Shutdown Supply Current Parameter and Endnote 7, Table 2 ... 4
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Deleted Terminal Voltage Operating Range Section and Figure 41, Renumbered Figures Sequentially ... 13
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5/03—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 kΩ VERSION

V_{DD} = 5 V ± 10%, or 3 V ± 10%; V_A = +V_{DD}; V_B = 0 V; −40°C < T_A < +125°C; unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS						
Rheostat Mode						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = no connect	−1.5	±0.1	+1.5	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = no connect	−4	±0.75	+4	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}	T_A = 25°C	−20		+20	%
Resistance Temperature Coefficient	$\Delta R_{AB}/\Delta T$	V_{AB} = V_{DD}, wiper = no connect		45		ppm/°C
Wiper Resistance	R_W			50	120	Ω
Potentiometer Divider Mode		Specifications apply to all VRs				
Resolution	N				8	Bits
Differential Nonlinearity[4]	DNL		−1.5	±0.1	+1.5	LSB
Integral Nonlinearity[4]	INL		−1.5	±0.6	+1.5	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 0x80		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0xFF	−6	−2.5	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	0	+2	+6	LSB
RESISTOR TERMINALS						
Voltage Range[5]	V_A, V_B, V_W		GND		V_{DD}	V
Capacitance A, Capacitance B[6]	$C_{A,B}$	f = 1 MHz, measured to GND, code = 0x80		45		pF
Capacitance W[6]	C_W	f = 1 MHz, measured to GND, code = 0x80		60		pF
Common-Mode Leakage	I_{CM}	V_A = V_B = $V_{DD}/2$		1		nA
DIGITAL INPUTS						
Input Logic High	V_{IH}		2.4			V
Input Logic Low	V_{IL}				0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	$V_{DD\ RANGE}$		2.7		5.5	V
Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		3	8	µA
Power Dissipation[7]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V			0.2	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = +5 V ± 10%, code = midscale		±0.02	±0.05	%/%
DYNAMIC CHARACTERISTICS[6, 8]						
Bandwidth −3 dB	BW_5K	R_{AB} = 5 kΩ, code = 0x80		1.2		MHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz		0.05		%
V_W Settling Time	t_S	V_A = 5 V, V_B = 0 V, ±1 LSB error band		1		µs
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 2.5 kΩ		6		nV/√Hz

[1] Typical specifications represent average readings at +25°C and V_{DD} = 5 V.
[2] Resistor position nonlinearity error (R-INL) is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.
[3] V_{AB} = V_{DD}, wiper (V_W) = no connect.
[4] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output digital-to-analog converter (DAC). V_A = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other.
[6] Guaranteed by design and not subject to production test.
[7] P_{DISS} is calculated from (I_{DD} × V_{DD}). CMOS logic level inputs result in minimum power dissipation.
[8] All dynamic characteristics use V_{DD} = 5 V.

10 kΩ, 50 kΩ, 100 kΩ VERSIONS

V_{DD} = 5 V ± 10%, or 3 V ± 10%; V_A = V_{DD}; V_B = 0 V; −40°C < T_A < +125°C; unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS						
Rheostat Mode						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = no connect	−1	±0.1	+1	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = no connect	−2	±0.25	+2	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}	T_A = 25°C	−15		+15	%
Resistance Temperature Coefficient	$\Delta R_{AB}/\Delta T$	V_{AB} = V_{DD}, Wiper = no connect		45		ppm/°C
Wiper Resistance	R_W	V_{DD} = 5 V		50	120	Ω
Potentiometer Divider Mode		Specifications apply to all VRs				
Resolution	N				8	Bits
Differential Nonlinearity[4]	DNL		−1	±0.1	+1	LSB
Integral Nonlinearity[4]	INL		−1	±0.3	+1	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 0x80		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0xFF	−3	−1	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	0	1	3	LSB
RESISTOR TERMINALS						
Voltage Range[5]	$V_{A,B,W}$		GND		V_{DD}	V
Capacitance A, Capacitance B[6]	$C_{A,B}$	f = 1 MHz, measured to GND, code = 0x80		45		pF
Capacitance W[6]	C_W	f = 1 MHz, measured to GND, code = 0x80		60		pF
Common-Mode Leakage	I_{CM}	V_A = V_B = V_{DD}/2		1		nA
DIGITAL INPUTS						
Input Logic High	V_{IH}		2.4			V
Input Logic Low	V_{IL}				0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	$V_{DD\ RANGE}$		2.7		5.5	V
Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		3	8	µA
Power Dissipation[7]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V			0.2	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = +5 V ± 10%, code = midscale		±0.02	±0.05	%/%
DYNAMIC CHARACTERISTICS[6, 8]						
Bandwidth −3 dB	BW	R_{AB} = 10 kΩ/50 kΩ/100 kΩ, Code = 0x80		600/100/40		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz, R_{AB} = 10 kΩ		0.05		%
V_W Settling Time (10 kΩ/50 kΩ/100 kΩ)	t_S	V_A = 5 V, V_B = 0 V, ±1 LSB error band		2		µs
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 5 kΩ		9		nV/√Hz

[1] Typical specifications represent average readings at +25°C and V_{DD} = 5 V.
[2] Resistor position nonlinearity error (R-INL) is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.
[3] V_{AB} = V_{DD}, wiper (V_W) = no connect.
[4] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output digital-to-analog converter (DAC). V_A = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other.
[6] Guaranteed by design and not subject to production test.
[7] P_{DISS} is calculated from (I_{DD} × V_{DD}). CMOS logic level inputs result in minimum power dissipation.
[8] All dynamic characteristics use V_{DD} = 5 V.

TIMING CHARACTERISTICS—ALL VERSIONS

V_{DD} = +5V ± 10%, or +3V ± 10%; V_A = V_{DD}; V_B = 0 V; −40°C < T_A < +125°C; unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
SPI INTERFACE TIMING CHARACTERISTICS[1, 2]		Specifications apply to all parts				
Clock Frequency	f_{CLK}				25	MHz
Input Clock Pulse Width	t_{CH}, t_{CL}	Clock level high or low	20			ns
Data Setup Time	t_{DS}		5			ns
Data Hold Time	t_{DH}		5			ns
$\overline{CS}$ Setup Time	t_{CSS}		15			ns
$\overline{CS}$ High Pulse Width	t_{CSW}		40			ns
CLK Fall to $\overline{CS}$ Fall Hold Time	t_{CSH0}		0			ns
CLK Fall to $\overline{CS}$ Rise Hold Time	t_{CSH1}		0			ns

[1] See the timing diagram, Figure 38, for location of measured values. All input control voltages are specified with t_R = t_F = 2 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.
[2] Guaranteed by design and not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C, unless otherwise noted.

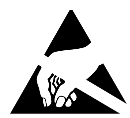
Table 4.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_A, V_B, V_W to GND	V_{DD}
Maximum Current I_{MAX}[1]	
I_{WB}, I_{WA} Pulsed	±20 mA
I_{WB}, I_{WA} Continuous	
5 kΩ, 10 kΩ	4.7 mA
50 kΩ	0.95 mA
100 kΩ	0.48 mA
Digital Inputs and Output Voltage to GND	0 V to +7 V
Temperature	
Operating Temperature Range	−40°C to +125°C
Maximum Junction Temperature (T_{JMAX})	150°C
Storage Temperature	−65°C to +150°C
Thermal Resistance (SOT-23 Package)[2]	
θ_{JA} Thermal Impedance	206°C/W
θ_{JC} Thermal Impedance	91°C/W
Reflow Soldering (Pb-Free)	
Peak Temperature	260°C
Time at Peak Temperature	10 sec to 40 sec

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and applied voltage across any two of the A, B, and W terminals at a given resistance.
[2] Package power dissipation = $(T_{JMAX} − T_A)/\theta_{JA}$.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

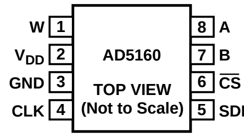


Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin	Mnemonic	Description
1	W	W Terminal.
2	V_{DD}	Positive Power Supply.
3	GND	Digital Ground.
4	CLK	Serial Clock Input. Positive edge triggered.
5	SDI	Serial Data Input.
6	$\overline{CS}$	Chip Select Input, Active Low. When $\overline{CS}$ returns high, data loads into the DAC register.
7	B	B Terminal.
8	A	A Terminal.

TYPICAL PERFORMANCE CHARACTERISTICS

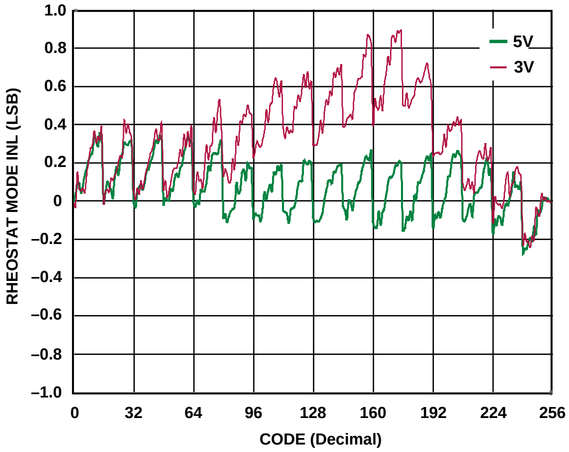


Figure 4. R-INL vs. Code vs. Supply Voltages

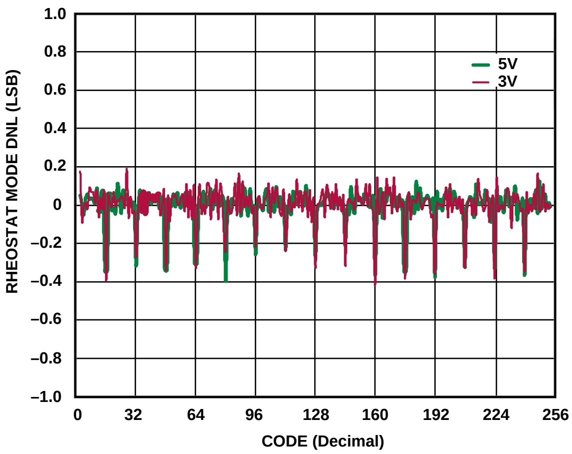


Figure 5. R-DNL vs. Code vs. Supply Voltages

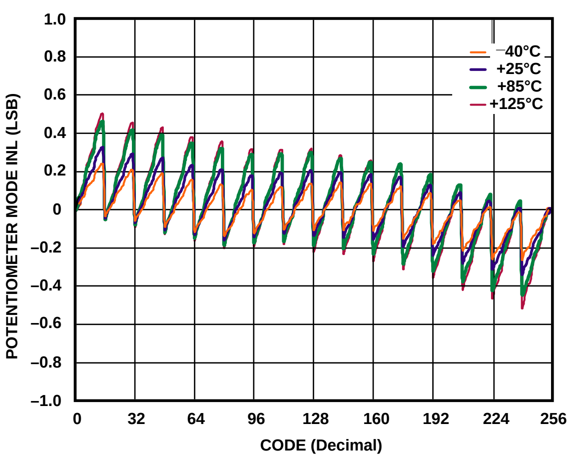


Figure 6. INL vs. Code, V_{DD} = 5 V

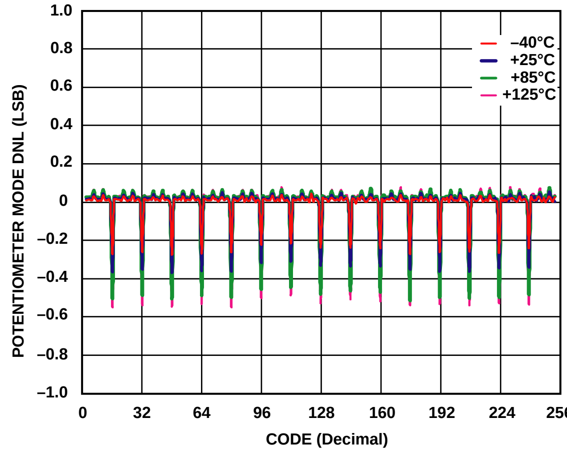


Figure 7. DNL vs. Code, V_{DD} = 5 V

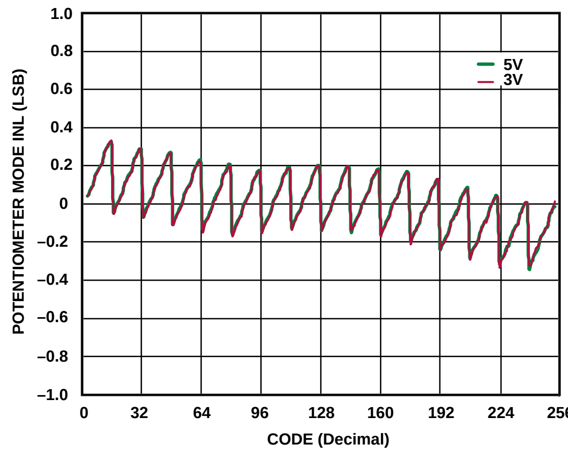


Figure 8. INL vs. Code vs. Supply Voltages

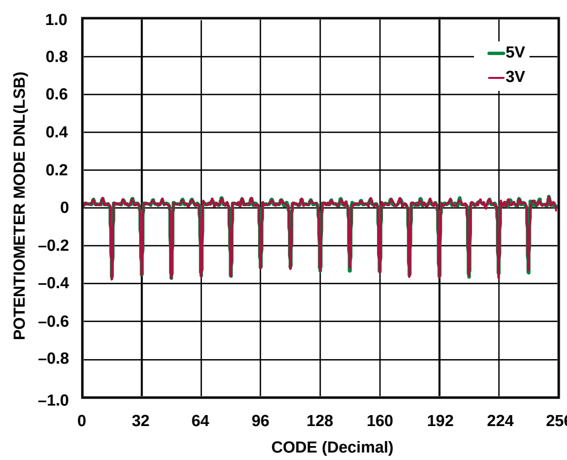


Figure 9. DNL vs. Code vs. Supply Voltages

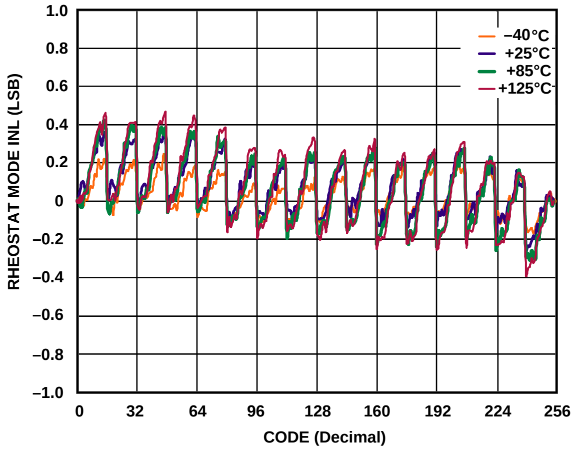


Figure 10. R-INL vs. Code, V_{DD} = 5 V

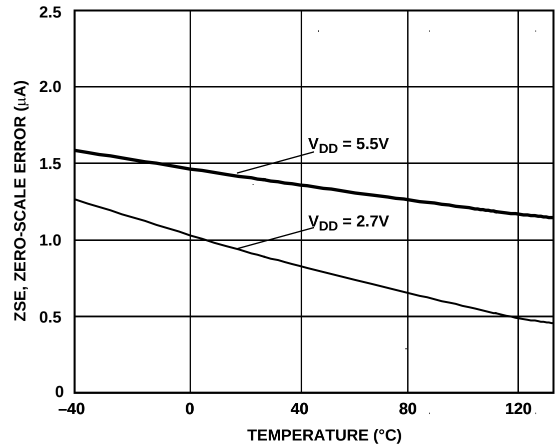


Figure 13. Zero-Scale Error vs. Temperature

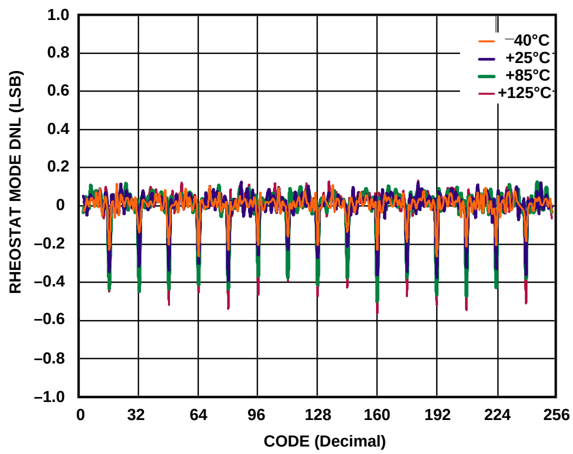


Figure 11. R-DNL vs. Code, V_{DD} = 5 V

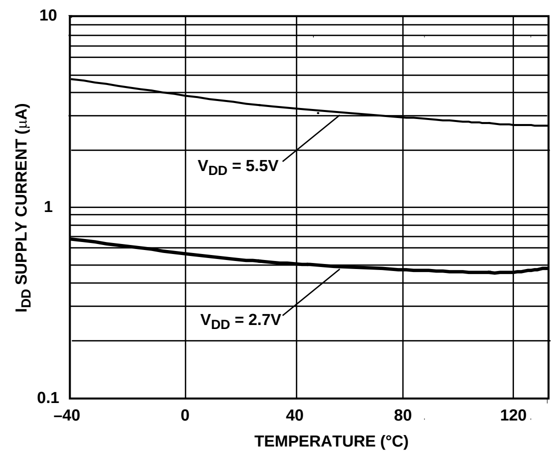


Figure 14. Supply Current vs. Temperature

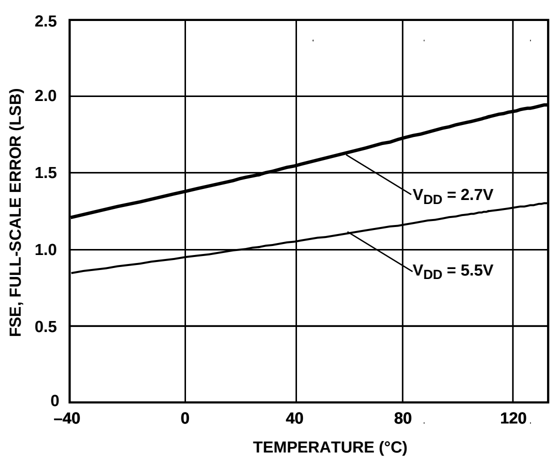


Figure 12. Full-Scale Error vs. Temperature

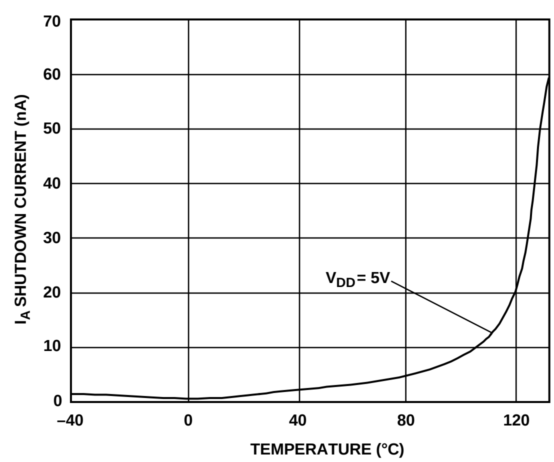


Figure 15. Shutdown Current vs. Temperature

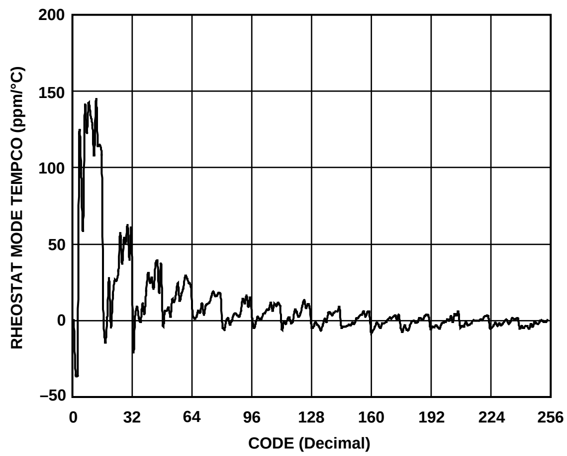


Figure 16. Rheostat Mode Tempco $\Delta R_{WB}/\Delta T$ vs. Code

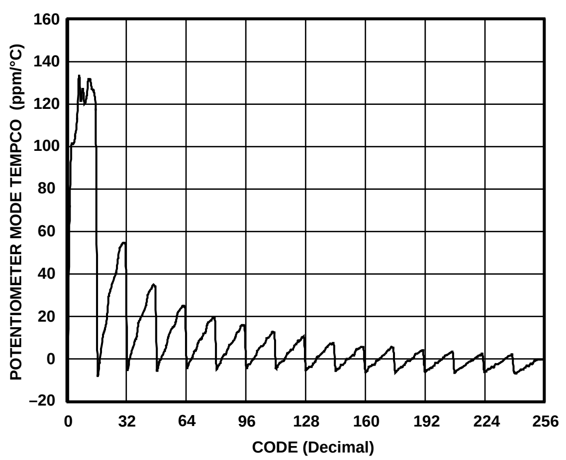


Figure 17. Potentiometer Mode Tempco $\Delta V_{WB}/\Delta T$ vs. Code

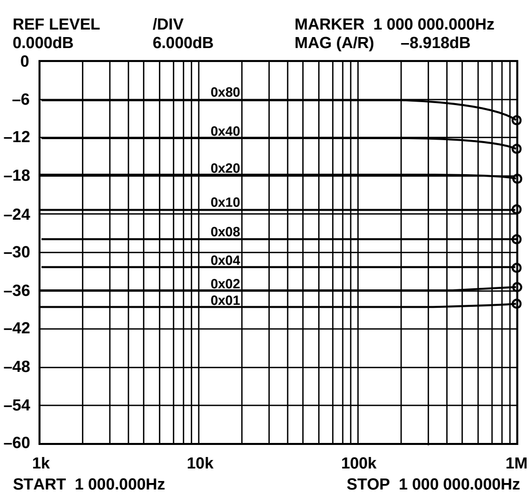


Figure 18. Gain vs. Frequency vs. Code, R_{AB} = 5 kΩ

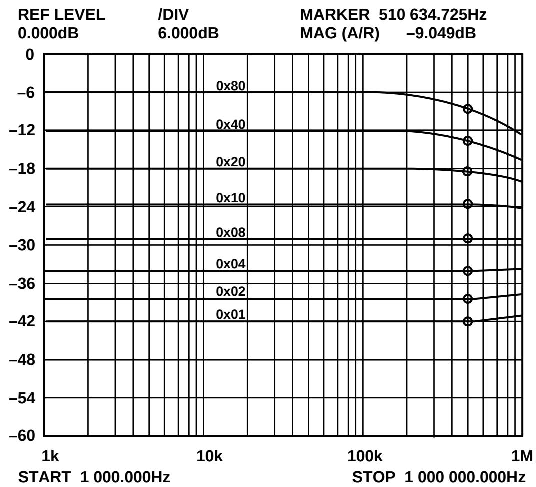


Figure 19. Gain vs. Frequency vs. Code, R_{AB} = 10 kΩ

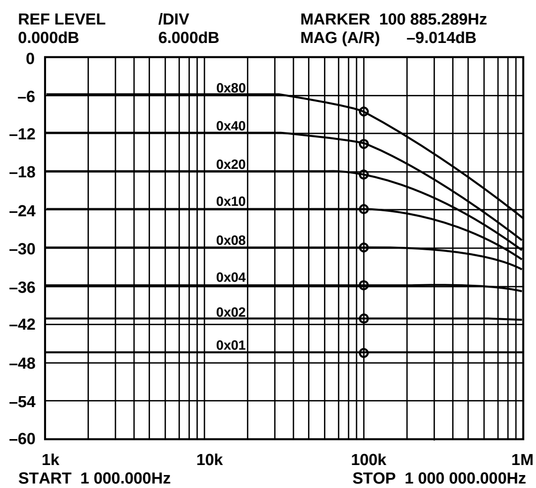


Figure 20. Gain vs. Frequency vs. Code, R_{AB} = 50 kΩ

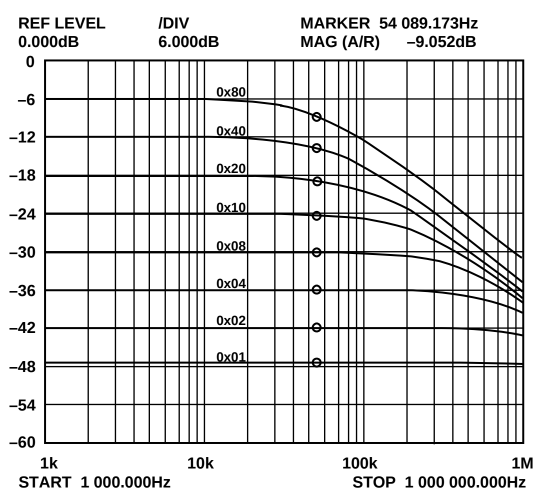


Figure 21. Gain vs. Frequency vs. Code, R_{AB} = 100 kΩ

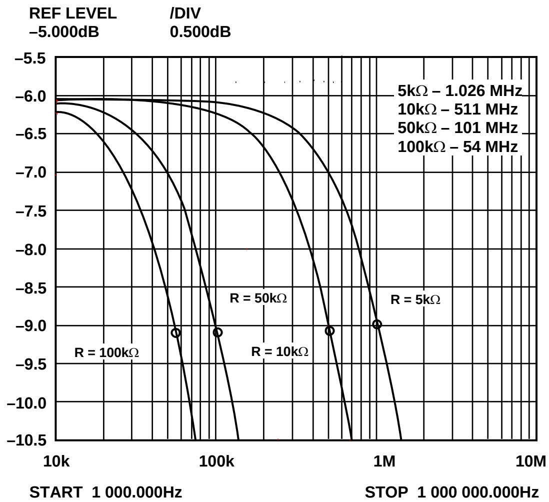


Figure 22. –3 dB Bandwidth @ Code = 0x80

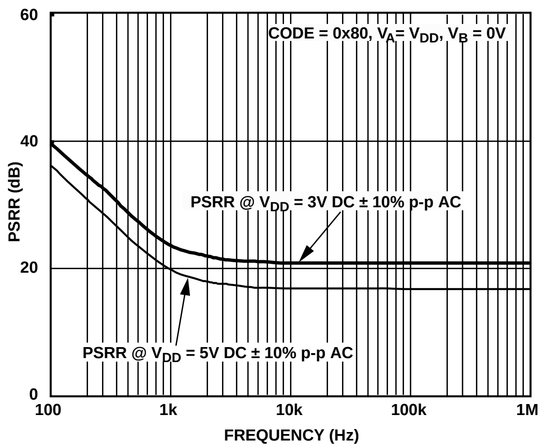


Figure 23. PSRR vs. Frequency

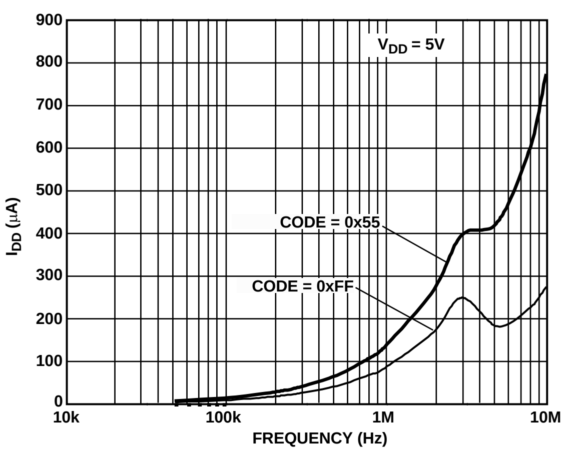


Figure 24. I_{DD} vs. Frequency

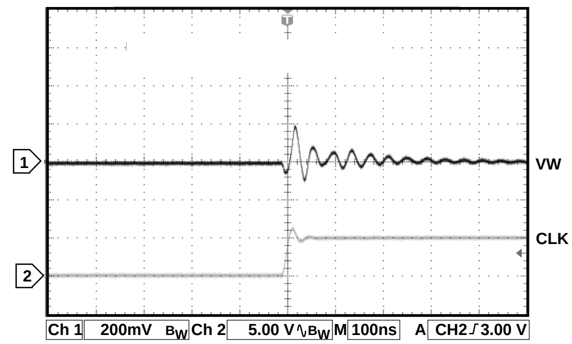


Figure 25. Digital Feedthrough

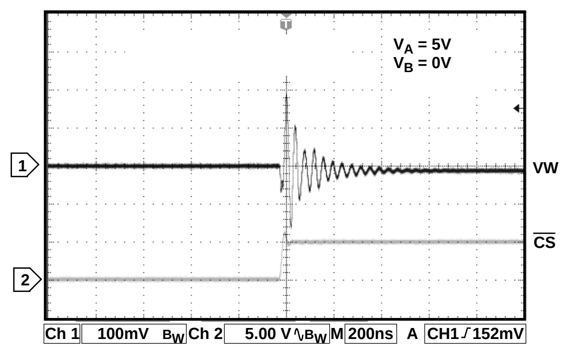


Figure 26. Midscale Glitch, Code 0x80 to Code 0x7F

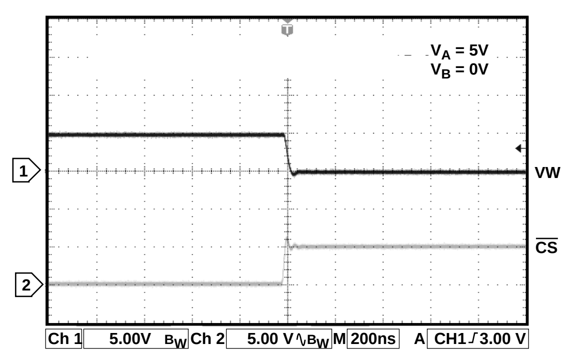


Figure 27. Large Signal Settling Time, Code 0xFF to Code 0x00

TEST CIRCUITS

Figure 28 to Figure 36 illustrate the test circuits that define the test conditions used in the product specification tables.

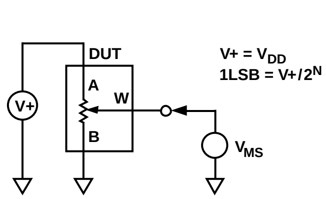


Figure 28. Test Circuit for Potentiometer Divider Nonlinearity Error (INL, DNL)

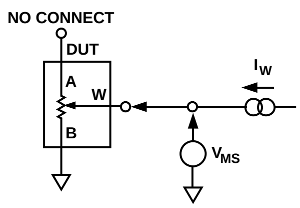


Figure 29. Test Circuit for Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

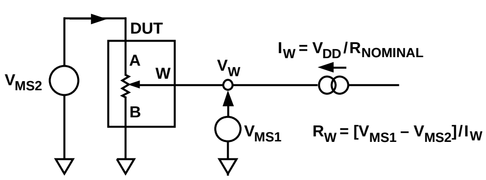


Figure 30. Test Circuit for Wiper Resistance

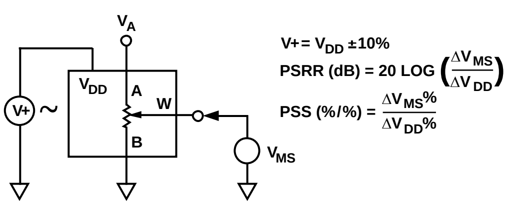


Figure 31. Test Circuit for Power Supply Sensitivity (PSS, PSSR)

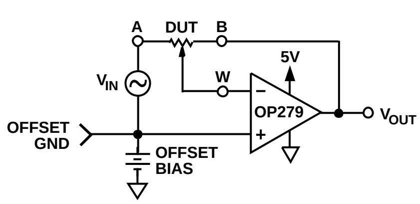


Figure 32. Test Circuit for Inverting Gain

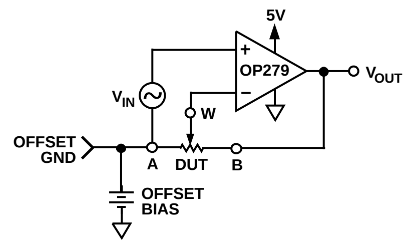


Figure 33. Test Circuit for Noninverting Gain

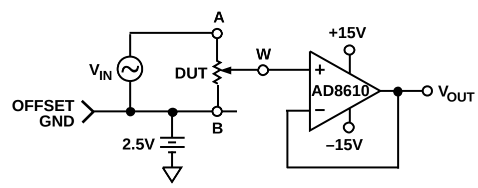


Figure 34. Test Circuit for Gain vs. Frequency

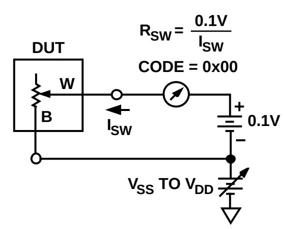


Figure 35. Test Circuit for Incremental On Resistance

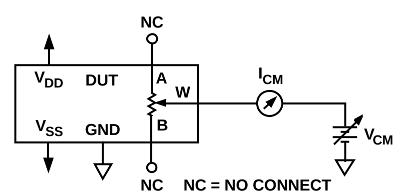


Figure 36. Test Circuit for Common-Mode Leakage Current

SPI INTERFACE

Table 6. Serial Data-Word Format

B7	B6	B5	B4	B3	B2	B1	B0
D7 MSB 2^7	D6	D5	D4	D3	D2	D1	D0 LSB 2^0

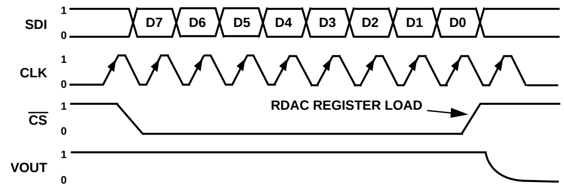


Figure 37. SPI Interface Timing Diagram (V_A = 5 V, V_B = 0 V, V_W = V_{OUT})

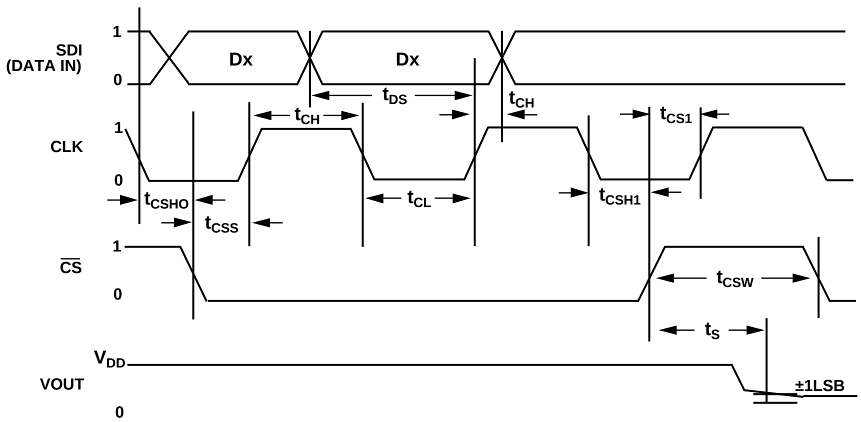


Figure 38. SPI Interface Detailed Timing Diagram (V_A = 5 V, V_B = 0 V, V_W = V_{OUT})

THEORY OF OPERATION

The AD5160 is a 256-position digitally controlled variable resistor (VR) device.

An internal power-on preset places the wiper at midscale during power-on, which simplifies the fault condition recovery at power-up.

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation

The nominal resistance of the RDAC between Terminal A and Terminal B is available in 5 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ. The final two or three digits of the model number as listed in the Ordering Guide section determine the nominal resistance value, for example, in model AD5160BRJZ10, the 10 represents 10 kΩ; and in AD5160BRJZ50, the 50 represents 50 kΩ.

The nominal resistance (R_{AB}) of the VR has 256 contact points accessed by the wiper terminal, plus the B terminal contact. The 8-bit data in the RDAC latch is decoded to select one of the 256 possible settings.

Assuming a 10 kΩ part is used, the first connection of the wiper starts at the B terminal for Data 0x00. Because there is a 60 Ω wiper contact resistance, such connection yields a minimum of 60 Ω resistance between Terminal W and Terminal B.

The second connection is the first tap point, which corresponds to 99 Ω ($R_{WB} = R_{AB}/256 + R_W = 39\ \Omega + 60\ \Omega$) for Data 0x01.

The third connection is the next tap point, representing 138 Ω (2 × 39 Ω + 60 Ω) for Data 0x02, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 9961 Ω (R_{AB} – 1 LSB + R_W). Figure 39 shows a simplified diagram of the equivalent RDAC circuit where the last resistor string is not accessed; therefore, there is 1 LSB less of the nominal resistance at full scale in addition to the wiper resistance.

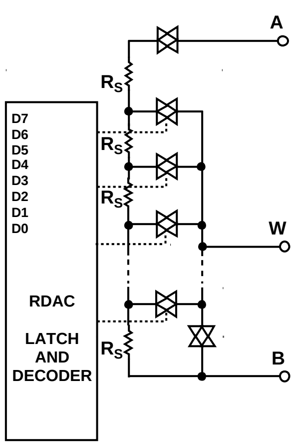


Figure 39. Equivalent RDAC Circuit

The general equation determining the digitally programmed output resistance between W and B is

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + R_W \quad (1)$$

where:
D is the decimal equivalent of the binary code loaded in the 8-bit RDAC register.
R_{AB} is the end-to-end resistance.
R_W is the wiper resistance contributed by the on resistance of the internal switch.

In summary, if R_{AB} = 10 kΩ and the A terminal is open circuited, the following output resistance R_{WB} is set for the indicated RDAC latch codes.

Table 7. Codes and Corresponding R_{WB} Resistance

D (Dec.)	R_{WB} (Ω)	Output State
255	9961	Full Scale (R_{AB} – 1 LSB + R_W)
128	5060	Midscale
1	99	1 LSB
0	60	Zero Scale (Wiper Contact Resistance)

Note that in the zero-scale condition, a finite wiper resistance of 60 Ω is present. Take care to limit the current flow between W and B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the Wiper W and Terminal A also produces a digitally controlled complementary resistance (R_{WA}). When these terminals are used, the B terminal can be opened. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{256 - D}{256} \times R_{AB} + R_W \quad (2)$$

For R_{AB} = 10 kΩ and the B terminal is open circuited, the following output resistance R_{WA} is set for the indicated RDAC latch codes.

Table 8. Codes and Corresponding R_{WA} Resistance

D (Dec.)	R_{WA} (Ω)	Output State
255	99	Full Scale
128	5060	Midscale
1	9961	1 LSB
0	10,060	Zero Scale

Typical device-to-device matching is process lot dependent and may vary by up to ±30%. Because the resistance element is processed in thin film technology, the change in R_{AB} with temperature has a very low 45 ppm/°C temperature coefficient.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates a voltage divider at wiper-to-B and wiper-to-A proportional to the input voltage at A-to-B. Unlike the polarity of V_{DD} to GND, which must be positive, voltage across A to B, W to A, and W to B can be at either polarity.

If ignoring the effect of the wiper resistance for approximation, connecting the A terminal to 5 V and the B terminal to ground produces an output voltage at the wiper-to-B starting at 0 V up to 1 LSB less than 5 V. Each LSB of voltage is equal to the voltage applied across Terminal A and Terminal B divided by the 256 positions of the potentiometer divider. The general equation defining the output voltage at V_W with respect to ground for any valid input voltage applied to Terminal A and Terminal B is

$$V_W(D) = \frac{D}{256}V_A + \frac{256-D}{256}V_B \quad (3)$$

For a more accurate calculation, which includes the effect of wiper resistance, V_W can be found as

$$V_W(D) = \frac{R_{WB}(D)}{256}V_A + \frac{R_{WA}(D)}{256}V_B \quad (4)$$

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. Unlike the rheostat mode, the output voltage is dependent mainly on the ratio of the internal resistors (R_{WA} and R_{WB}) and not the absolute values. Therefore, the temperature drift reduces to 15 ppm/°C.

SPI-COMPATIBLE 3-WIRE SERIAL BUS

The AD5160 contains a 3-wire SPI-compatible digital interface (SDI, $\overline{CS}$, and CLK). The 8-bit serial word must be loaded MSB first. The format of the word is shown in Table 6.

The positive-edge sensitive CLK input requires clean transitions to avoid clocking incorrect data into the serial input register. Standard logic families work well. If mechanical switches are used for product evaluation, they should be debounced by a flip-flop or other suitable means. When $\overline{CS}$ is low, the clock loads data into the serial register on each positive clock edge (see Figure 37).

The data setup and data hold times in the specification table determine the valid timing requirements. The AD5160 uses an 8-bit serial input data register word that is transferred to the internal RDAC register when the $\overline{CS}$ line returns to logic high. Extra MSB bits are ignored.

ESD PROTECTION

All digital inputs are protected with a series input resistor and parallel Zener ESD structures are shown in Figure 40 and Figure 41. This applies to SDI, CLK, and $\overline{CS}$, which are the digital input pins.

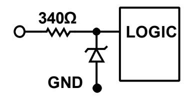


Figure 40. ESD Protection of Digital Pins

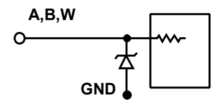


Figure 41. ESD Protection of Resistor Terminals

POWER-UP SEQUENCE

Because the ESD protection diodes limit the voltage compliance at the A, B, and W terminals, it is important to power V_{DD}/GND before applying any voltage to the A, B, and W terminals; otherwise, the diode forward biases such that V_{DD} is powered unintentionally and may affect the rest of the user's circuit. The ideal power-up sequence is in the following order: GND, V_{DD}, digital inputs, and then $V_{A/B/W}$. The relative order of powering V_A, V_B, V_W, and the digital inputs is not important as long as they are powered after V_{DD}/GND.

LAYOUT AND POWER SUPPLY BYPASSING

It is a good practice to employ compact, minimum lead length layout design. Keep the leads to the inputs as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also a good practice to bypass the power supplies with quality capacitors for optimum stability. Bypass supply leads to the device with disc or chip ceramic capacitors of 0.01 µF to 0.1 µF. To minimize any transient disturbance and low frequency ripple, apply low ESR 1 µF to 10 µF tantalum or electrolytic capacitors at the supplies (see Figure 42). To minimize the ground bounce, join the digital ground remotely to the analog ground at a single point.

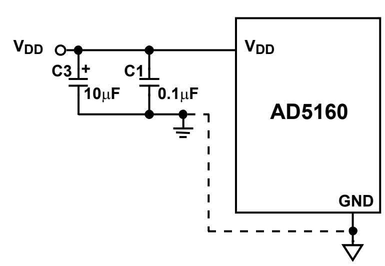


Figure 42. Power Supply Bypassing

OUTLINE DIMENSIONS

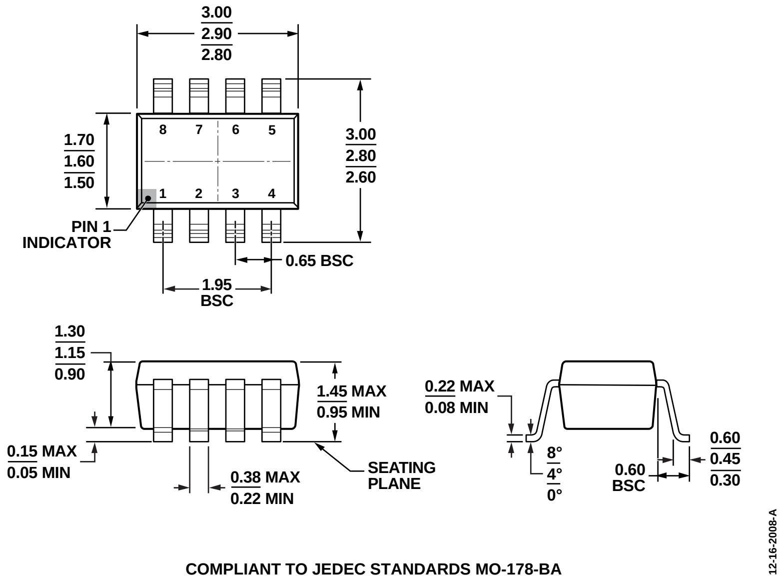


Figure 43. 8-Lead Small Outline Transistor Package [SOT-23] (RJ-8) Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2, 3]	R_{AB} (Ω)	Temperature	Package Description	Package Option	Branding
AD5160BRJZ5-R2	5 k	−40°C to +125°C	8-Lead SOT-23	RJ-8	D6Q
AD5160BRJZ5-RL7	5 k	−40°C to +125°C	8-Lead SOT-23	RJ-8	D6Q
AD5160BRJZ10-R2	10 k	−40°C to +125°C	8-Lead SOT-23	RJ-8	D09
AD5160BRJZ10-RL7	10 k	−40°C to +125°C	8-Lead SOT-23	RJ-8	D09
AD5160BRJZ50-R2	50 k	−40°C to +125°C	8-Lead SOT-23	RJ-8	D8J
AD5160BRJZ50-RL7	50 k	−40°C to +125°C	8-Lead SOT-23	RJ-8	D8J
AD5160BRJZ100-R2	100 k	−40°C to +125°C	8-Lead SOT-23	RJ-8	D0B
AD5160BRJZ100-RL7	100 k	−40°C to +125°C	8-Lead SOT-23	RJ-8	D0B
EVAL-AD5160DBZ			Evaluation Board		

[1] The AD5160 contains 2532 transistors. Die size: 30.7 mil × 76.8 mil = 2358 sq. mil.
[2] Z = RoHS Compliant Part.
[3] The EVAL-AD5160DBZ board is shipped with the 10 kΩ R_{AB} resistor option; however, the board is compatible with all available resistor value options.