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Keywords: HDLC Controller, DS31256

APPLICATION NOTE 2867

Initialization Steps for the DS31256

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Abstract: The recommended initialization sequences for DS31256 Envoy HDLC controller before sending packet data.

Introduction

By design, upon power-up the DS31256 will not take control of the PCI bus. All the physical ports (ports 0 to 15) send all ones (not HDLC idle code), therefore placing the DS31256 in an idle upon power-up. On the other hand, the DS31256 can initialize RAM base memory, both direct and indirect, to store states of the internal state machines. There are many very complex state machines and interworking functional blocks of the DS31256, therefore upon power-up all of these internal registers/RAMs must be initialized to a known state before any data packets can be transmitted and received. It is suggested that users follow the initialization sequence steps in Table 1 before sending packet data.

Table 1. Initialization Sequence Steps for the DS31256

| Initialization Step | Comments |
|---|--|
| 1. System reset. | System reset can be invoked by either hardware action via the PRST-bar signal or software action via the RST control bit in the Master Reset and ID register; all the internal device configuration registers are set to zero (0000h). |
| 2. Configure Local Bus Bridge Mode Control register (LBBMC), if DS31256 is used in bridge mode. | Please note that these registers are not affected by a software-invoked system reset. It will be forced to all zeros only by hardware reset. |
| 3. Initialize the PCI configuration registers. | Achieved by asserting the PIDSEL signal. |
| 4. Master software reset. | Master software reset in MRID register. |
| 5. Initialize all indirect registers to zero. | It is recommended that all the indirect registers be set to 0000h. See Table 2 for a list of all indirect registers. |
| 6. Master software reset. | Master software reset in MRID register. |
| 7. Configure the device for operation. | Program all the necessary registers, which includes the Layer One, HDLC, FIFO, and DMA registers, but except: <ol style="list-style-type: none"> 1. Ports are disabled; keep layer-one ports off by leaving the TFDA1 bits to 0 (default state) in TP[n]CR register. 2. HDLC channels are disabled. 3. DMA and DMA channels are disabled. 4. In high-speed unchannelized mode, set it to low-speed unchannelized mode in the RP[n]CR register and enable it to high-speed unchannelized mode in Step 12 (see below). |
| 8. Enable the HDLC channels. | Done via the RCHEN and TCHEN bits in the R[n]CFG[j] and T[n]CFG[j] registers. |
| 9. Load the DMA descriptors. | Indicate to the DMA where packet data can be written and where pending data (if any) resides. |
| 10. Enable the DMAs. | Done via the RDE and TDE control bits in the Master Configuration (MC) register. |
| 11. Enable DMA for each HDLC channel. | Done via the channel-enable bit in the receive and transmit configuration RAM. |
| 12. Turns on HDLC channels. | Enable and allow ports to transmit normally, set TFDA1 bits to 1 in TP[n]CR registers. Note: For high-speed unchannelized mode only, enable high-speed unchannelized in RP[n]CR register. |
| 13. Wait enough time for all configurations to take effect. | It is going to take a minimum of 500µs or 768 RC and TC clock cycles (which ever is longer) before packet data can be processed. |

Note: It is recommended that a "Hardware Reset" be applied to the DS31256 upon power-on.

Table 2. Indirect Registers

| Offset/Address | Register Name | Number of Indirect Registers | Data Sheet Section |
|----------------|--|---|--------------------|
| 0x3xx | Channelized Port Data Indirect Select (CP0RDIS to CP15RDIS) | 6144 (16 Ports x 128 DS0 Channels x 3 Registers for each DS0 Channel) | 6.3 |
| 0x400 | Receive HDLC Channel Definition Indirect Select (RHCDIS) | 256 (one for each HDLC Channel) | 7.2 |
| 0x480 | Transmit HDLC Channel Definition Indirect Select (THCDIS) | 256 (one for each HDLC Channel) | 7.2 |
| 0x770 | Receive DMA Configuration Indirect Select (RDMACIS) | 1536 (one for each HDLC Channel) | 9.3.5 |
| 0x870 | Transmit DMA Configuration Indirect Select (TDMACIS) | 3072 (one for each HDLC Channel) | 9.3.5 |
| 0x900 | Receive FIFO Staring Block Pointer Indirect Select (RFSBPIS) | 256 (one for each HDLC Channel) | 8.2 |
| 0x910 | Receive FIFO Block Pointer Indirect Select (RFBPIS) | 1024 (one for each FIFO Block) | 8.2 |
| 0x920 | Receive FIFO High Watermark Indirect Select (RFHWMIS) | 256 (one for each HDLC Channel) | 8.2 |
| 0x980 | Transmit FIFO Staring Block Pointer (TFSBPIS) | 256 (one for each HDLC Channel) | 8.2 |
| 0x990 | Transmit FIFO Block Pointer Indirect Select (TFBPIS) | 1024 (one for each FIFO Block) | 8.2 |
| 0x9A0 | Transmit FIFO Low Watermark Indirect Select (TFLWMIS) | 256 (one for each HDLC Channel) | 8.2 |

Conclusion

This application note has shown how to initial the DS31256 in sequence, before any data packets can be transmitted and received.

If you have further questions about our HDLC controller products, please contact the [Telecommunication Applications support team](#).

Related Parts

[DS31256](#)

256-Channel, High-Throughput HDLC Controller

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