8 – 18V_{IN}, 15A ZVS Buck Regulator

Product Description

The PI34xx-00 is a family of high-efficiency DC-DC ZVS Buck regulators integrating the controller, power switches and support components within a high-density System-in-Package (SiP).

The PI34xx-00 is designed to achieve optimum efficiency at low input voltage ranges (8 – 18V). The utilization of zero-current soft turn-on provided by the high-performance ZVS topology within the PI34xx-00 series increases point-of-load performance, providing best in class power efficiency with high throughput power.

The PI34xx-00 requires only an external inductor and minimal capacitors to form a complete DC-DC switching-mode buck regulator.

Device	Output Voltage		I_{OUT} Max
	Set	Range	
PI3423-00-LGIZ	3.3V	2.3 – 4.1V	15A
PI3424-00-LGIZ	5.0V	3.3 – 6.5V	15A

The ZVS architecture enables high-frequency operation while minimizing switching losses and maximizing efficiency. The high-switching-frequency operation reduces the size of the external filtering components, improves power density, and enables very fast dynamic response to line and load transients.

The ZVS architecture enables operation up to 750kHz while minimizing switching losses and the use of variable frequency extends high efficiency over a very wide dynamic range. The PI34xx-00 series has a minimum on time of 20ns which enables large step-down conversion ratios.

Features & Benefits

- High-efficiency ZVS Buck topology
- Input voltage range of 8 – 18V
- Very fast transient response
- Power-up into pre-biased load
- High-accuracy pre-trimmed output voltage
- User adjustable soft start & tracking
- Parallel capable with single-wire current sharing
- Input over/undervoltage lockout (OVLO/UVLO)
- Output overvoltage protection (OVP)
- Overtemperature Protection (OTP)
- Fast and slow current limits
- –40 to 125°C operating range (T_{INT})

Applications

- High-Efficiency Systems
- Computing, Communications, Industrial, Automotive Equipment

Package Information

- 10 x 14 x 2.6mm LGA SiP

Note: Product images may not highlight current product markings.

Contents

Order Information

Product	Output Range		I_{OUT} Max	Package	Transport Media
	Set	Range			
PI3423-00-LGIZ	3.3V	2.3 – 4.1V	15A	10 x 14mm 123-pin LGA	TRAY
PI3424-00-LGIZ	5.0V	3.3 – 6.5V	15A	10 x 14mm 123-pin LGA	TRAY

Thermal, Storage and Handling Information

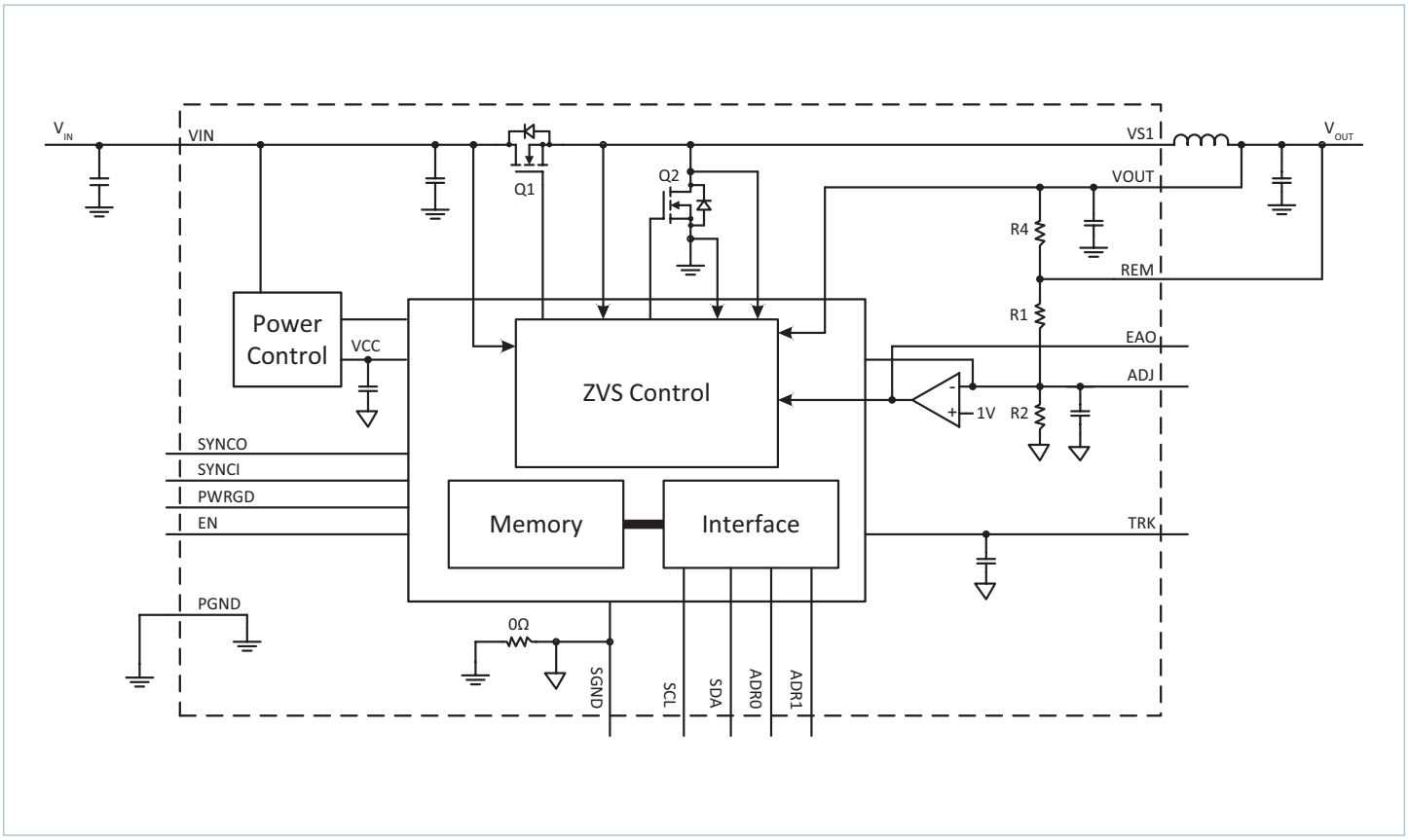
Name	Rating
Storage Temperature	–65 to 150°C
Internal Operating Temperature	–40 to 125°C
Soldering Temperature for 20 seconds	245°C
MSL Rating	3
ESD Rating	2kV HBM; 1.0kV CDM

Absolute Maximum Ratings

Name	Rating
VIN	–0.7 to 22V
VS1	–0.7 to 22V, 25V for 5ns, –4V for 5ns
VOUT, REM	**See relevant product section**
SGND	100mA
PWRGD, SYNCO, SYNCI, EN, EAO, ADJ, TRK, ADR1, ADR2, SCL, SDA, VDR	–0.3 to 5.5V / 5mA

Notes: At 25°C ambient temperature. Stresses beyond these limits may cause permanent damage to the device. Operation at these conditions or conditions beyond those listed in the Electrical Characteristics is not guaranteed. All voltage nodes are referenced to PGND unless otherwise noted. Test conditions are per the specifications within the individual product Electrical Characteristics.

Functional Block Diagram

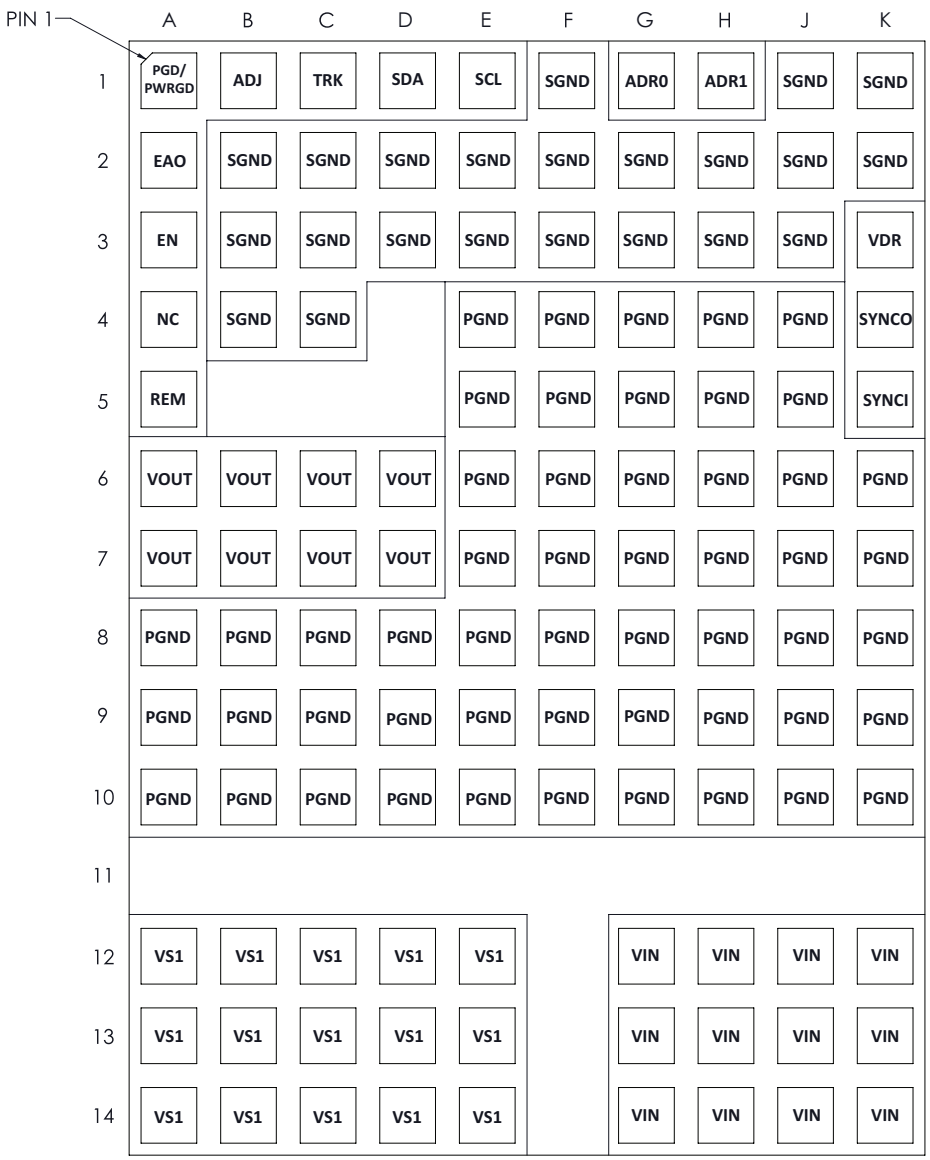


Simplified block diagram (I²C™ pins SCL, SDA, ADR0, and ADR1 are for factory use only. Not for use in application.)

Pin Description

Name	Location	I/O	Description
SGND	Block 1	I/O	**Signal Ground:** Internal logic ground for EA, TRK, SYNCI, SYNCO and ADJ. SGND and PGND are star-connected within the regulator package.
PGND	Block 2	Power	**Power Ground:** VIN and VOUT power returns.
VIN	Block 3	Power	**Input Voltage:** and sense for UVLO, OVLO and feed-forward ramp.
VOUT	Block 5	Power	**Output Voltage:** and sense for power switches and feed-forward ramp.
VS1	Block 4	Power	**Switching Node:** and ZVS sense for power switches.
PWRGD	A1	O	**Power Good:** High-impedance when regulator is operating and output voltage is within approximately 80% of regulation set point; also can be used for parallel timing manangement intended for lead regulator.
EAO	A2	O	**Error Amp Output:** External connection for additional compensation and current sharing.
EN	A3	I/O	**Enable Input:** Regulator enable control. Asserted high or left floating: regulator enabled. Asserted low: regulator output disabled.
REM	A5	I	**Remote Sense:** High-side connection. Connect to output regulation point.
ADJ	B1	I	**Adjust Input:** An external resistor may be connected between ADJ pin and SGND or VOUT to trim the output voltage up or down.
TRK	C1	I/O	**Soft-Start and Track Input:** An external capacitor may be connected between TRK pin and SGND to decrease the rate of rise during soft start.
NC	A4	Open	**No Connect:** Leave pins floating.
SYNCO	K4	O	**Synchronization Output:** Outputs a high signal for ½ of the minimum period for synchronization of other regulators.
VDR	K3	O	Internally generated 5.1V for internal use. May be used externally provided it is impedance-limited to prevent current in excess of 2mA under any circumstances.
SYNCI	K5	I	**Synchronization Input:** Synchronize to the falling edge of external clock frequency. SYNCI is a high-impedance digital input node and should always be connected to SGND when not in use.
SDA	D1	I/O	**Data Line:** Connect to SGND. Factory use only. Not for use in application.
SCL	E1	I/O	**Clock Line:** Connect to SGND. Factory use only. Not for use in application.
ADR1	H1	I	**Tri-State Address:** No connect. Factory use only. Not for use in application.
ADR0	G1	I	**Tri-State Address:** No connect. Factory use only. Not for use in application.

Package Pinout



TOP THROUGH VIEW OF PRODUCT

PI34xx-00

Pin Block Name	Group of pins
SGND	B2-4, C2-4, D2-3, E2-3, F1-3, G2-3, H2-3, J1-3, K1-2
PGND	A8-10, B8-10, C8-10, D8-10, E4-10, F4-10, G4-10, H4-10, J4-10, K6-10
VIN	G12-14, H12-14, J12-14, K12-14
VS1	A12-14, B12-14, C12-14, D12-14, E12-14
VOUT	A6-7, B6-7, C6-7, D6-7

PI3423-00-LGIZ (3.3V_{OUT}) Electrical Characteristics

Specifications apply for –40°C < T_{INT} < 125°C, V_{IN} = 12V, L1 = 150nH [a] unless other conditions are noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Specifications						
Input Voltage	V_{IN_DC}	[f]	8	12	18	V
Input Current	I_{IN_DC}	V_{IN} = 12V, T_C = 25°C, I_{OUT} = 15A		4.43		A
Input Current at Output Short (Fault-Condition Duty Cycle)	I_{IN_Short}	[b]			10	mA
Input Quiescent Current	I_{Q_VIN}	Disabled		2.6		mA
		Enabled (no load)		4		
Input Voltage Slew Rate	V_{IN_SR}	[b]			1	V/µs
Output Specifications						
Output Voltage Total Regulation	V_{OUT_DC}	[b]	3.24	3.30	3.36	V
Output Voltage Trim Range	V_{OUT_DC}	[c]	2.3	3.3	4.1	V
Line Regulation	$\Delta V_{OUT}(\Delta V_{IN})$	At 25°C, 8V < V_{IN} < 18V		0.10		%
Load Regulation	$\Delta V_{OUT}(\Delta I_{OUT})$	At 25°C, 0.5A < I_{OUT} < 15A		0.10		%
Output Voltage Ripple	V_{OUT_AC}	I_{OUT} = 7.5A, C_{OUT} = 8 x 100µF, 20MHz BW [d]		17		mV_{P-P}
Continuous Output Current Range	I_{OUT_DC}	Refer to load current vs. ambient temperature curves			15	A
Current Limit	I_{OUT_CL}			18		A
Protection						
UVLO Start Threshold	V_{UVLO_START}		7.10	7.60	8.00	V
UVLO Stop Hysteresis	V_{UVLO_HYS}			0.36		V
OVLO Stop Threshold	V_{OVLO}		19.0	20.75	21.78	V
OVLO Start Hysteresis	V_{OVLO_HYS}			0.37		V
UVLO/OVLO Fault Delay Time	t_{f_DLY}	Number of the switching-frequency cycles		128		Cycles
UVLO/OVLO Response Time	t_f	+1% overdrive		500		ns
Output Overvoltage Protection	V_{OVP}	Above set V_{OUT}		20		%
Overtemperature Fault Threshold	T_{OTP}		130	135	140	°C
Overtemperature Restart Hysteresis	T_{OTP_HYS}			30		°C

[a] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI34xx-00 evaluation board with 3 x 4in dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[b] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control.
[c] Output current capability may be limited and other performance may vary from noted electrical characteristics when switching frequency or V_{OUT} is modified.
[d] Refer to output ripple plots.
[e] Refer to switching frequency vs. load current curves.
[f] Minimum 5V between V_{IN} – V_{OUT} must be maintained or a minimum load of 1mA required.

PI3423-00-LGIZ (3.3V_{OUT}) Electrical Characteristics (Cont.)

Specifications apply for –40°C < T_{INT} < 125°C, V_{IN} = 12V, L1 = 150nH [a] unless other conditions are noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Timing						
Switching Frequency	f_S	[e]		700		kHz
Fault Restart Delay	t_{FR_DLY}			30		ms
Sync In (SYNCI)						
Synchronization Frequency Range	Δf_{SYNCI}	Relative to set switching frequency [c]	50		110	%
SYNCI Threshold	V_{SYNCI}			2.5		V
SYNCI Input Impedance	Z_{SYNCI}			100		kΩ
Sync Out (SYNCO)						
SYNCO High	V_{SYNCO_HI}	Source 1mA	4.5			V
SYNCO Low	V_{SYNCO_LO}	Sink 1mA			0.5	V
SYNCO Rise Time	t_{SYNCO_RT}	20pF load		10		ns
SYNCO Fall Time	t_{SYNCO_FT}	20pF load		10		ns
Soft Start and Tracking						
TRK Active Input Range	V_{TRK}	Internal reference tracking range	0		1.2	V
TRK Max Output Voltage	V_{TRK_MAX}			1.2		V
TRK Enable Threshold	V_{TRK_OV}		20	40	62	mV
Charge Current (Soft–Start)	I_{TRK}		–70	–50	–25	µA
Discharge Current (Fault)	I_{TRK_DIS}			6.8		mA
Soft-Start Time	t_{SS}	C_{TRK} = 0µF		2.2		ms
TRK to EAIN Offset			34		100	mV
Enable						
High Threshold	V_{EN_HI}		0.9	1	1.1	V
Low Threshold	V_{EN_LO}		0.7	0.8	0.9	V
Threshold Hysteresis	V_{EN_HYS}		100	200	300	mV
Enable Pull-Up Voltage (Floating, Unfaulted)	V_{EN_PU}	With positive-logic EN polarity		2		V
Enable Pull-Down Voltage (Floating, Faulted)	V_{EN_PD}	With negative-logic EN polarity		0		V
Source Current	I_{EN_SO}	With positive-logic EN polarity		–50		µA
Sink Current	I_{EN_SK}	With negative-logic EN polarity		50		µA

[a] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI34xx-00 evaluation board with 3 x 4in dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[b] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control.
[c] Output current capability may be limited and other performance may vary from noted electrical characteristics when switching frequency or V_{OUT} is modified.
[d] Refer to output ripple plots.
[e] Refer to switching frequency vs. load current curves.
[f] Minimum 5V between V_{IN} – V_{OUT} must be maintained or a minimum load of 1mA required.

PI3423-00-LGIZ (3.3V_{OUT}) Electrical Characteristics (Cont.)

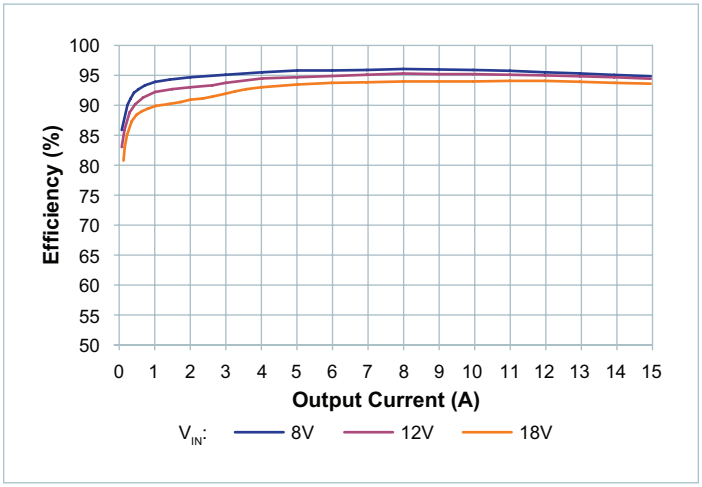


Figure 1 — *Efficiency at 25°C*

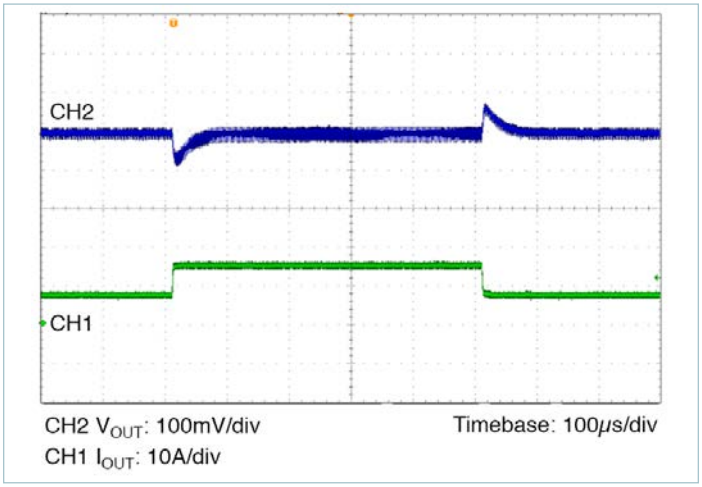


Figure 4 — *Transient response: 7.5 – 15A, at 5A/µs*

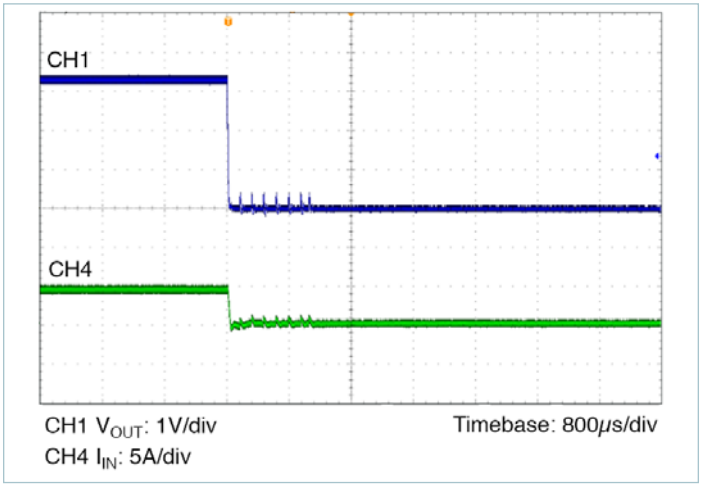


Figure 2 — *Short circuit test*

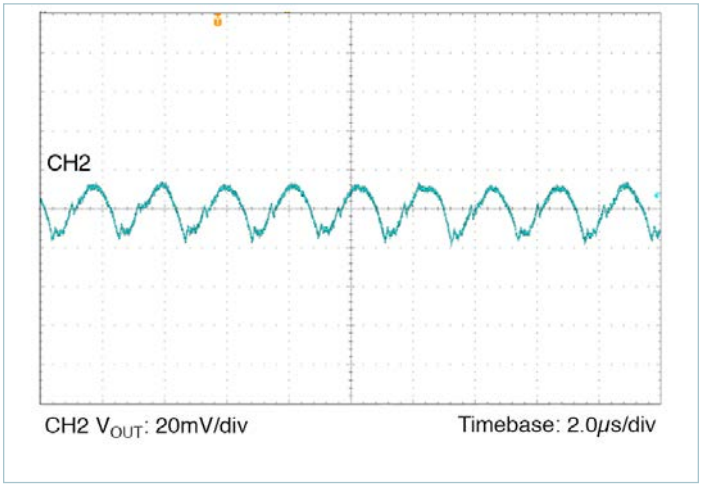


Figure 5 — *Output ripple 12V_{IN} 3.3V_{OUT} at 15A; C_{OUT} = 8 x 100µF*

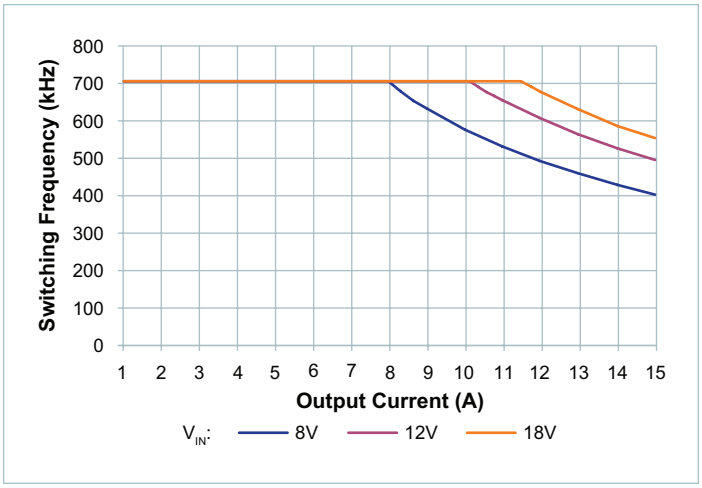


Figure 3 — *Switching frequency vs. load current*

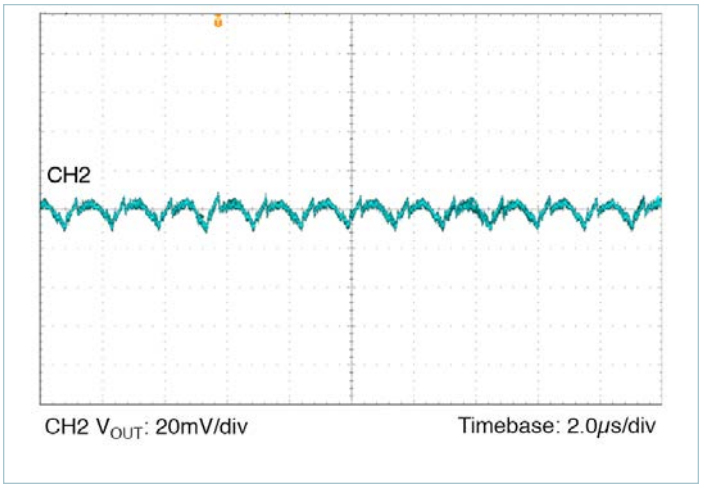


Figure 6 — *Output ripple 12V_{IN} 3.3V_{OUT} at 7.0A; C_{OUT} = 8 x 100µF*

PI3424-00-LGIZ (5.0V_{OUT}) Electrical Characteristics

Specifications apply for –40°C < T_{INT} < 125°C, V_{IN} = 12V, L1 = 150nH [a] unless other conditions are noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Specifications						
Input Voltage	V_{IN_DC}	[f]	8	12	18	V
Input Current	I_{IN_DC}	V_{IN} = 12V, T_C = 25°C, I_{OUT} = 15A		6.57		A
Input Current at Output Short (Fault-Condition Duty Cycle)	I_{IN_Short}	[b]			10	mA
Input Quiescent Current	I_{Q_VIN}	Disabled		2.6		mA
		Enabled (no load)		4		
Input Voltage Slew Rate	V_{IN_SR}	[b]			1	V/µs
Output Specifications						
Output Voltage Total Regulation	V_{OUT_DC}	[b]	4.93	5	5.07	V
Output Voltage Trim Range	V_{OUT_DC}	[c]	3.3		6.5	V
Line Regulation	$\Delta V_{OUT}(\Delta V_{IN})$	At 25°C, 8V < V_{IN} < 18V		0.10		%
Load Regulation	$\Delta V_{OUT}(\Delta I_{OUT})$	At 25°C, 0.5A < I_{OUT} < 15A		0.10		%
Output Voltage Ripple	V_{OUT_AC}	I_{OUT} = 7.5A, C_{OUT} = 8 x 100µF, 20MHz BW [d]		20.8		mV_{P-P}
Continuous Output Current Range	I_{OUT_DC}	Refer to load current vs. ambient temperature curves			15	A
Current Limit	I_{OUT_CL}			18		A
Protection						
UVLO Start Threshold	V_{UVLO_START}		7.10	7.60	8.00	V
UVLO Stop Hysteresis	V_{UVLO_HYS}			0.36		V
OVLO Stop Threshold	V_{OVLO}		19.0	20.75	21.78	V
OVLO Start Hysteresis	V_{OVLO_HYS}			0.37		V
UVLO/OVLO Fault Delay Time	t_{f_DLY}	Number of the switching-frequency cycles		128		Cycles
UVLO/OVLO Response Time	t_f	+1% overdrive		500		ns
Output Overvoltage Protection	V_{OVP}	Above set V_{OUT}		20		%
Overtemperature Fault Threshold	T_{OTP}		130	135	140	°C
Overtemperature Restart Hysteresis	T_{OTP_HYS}			30		°C

[a] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI34xx-00 evaluation board with 3 x 4in dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[b] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control.
[c] Output current capability may be limited and other performance may vary from noted electrical characteristics when switching frequency or V_{OUT} is modified.
[d] Refer to output ripple plots.
[e] Refer to switching frequency vs. load current curves.
[f] Minimum 5V between V_{IN} – V_{OUT} must be maintained or a minimum load of 1mA required.

PI3424-00-LGIZ (5.0V_{OUT}) Electrical Characteristics (Cont.)

Specifications apply for –40°C < T_{INT} < 125°C, V_{IN} = 12V, L1 = 150nH [a] unless other conditions are noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Timing						
Switching Frequency	f_S	[e]		750		kHz
Fault Restart Delay	t_{FR_DLY}			30		ms
Sync In (SYNCI)						
Synchronization Frequency Range	Δf_{SYNCI}	Relative to set switching frequency [c]	50		110	%
SYNCI Threshold	V_{SYNCI}			2.5		V
SYNCI Input Impedance	Z_{SYNCI}			100		kΩ
Sync Out (SYNCO)						
SYNCO High	V_{SYNCO_HI}	Source 1mA	4.5			V
SYNCO Low	V_{SYNCO_LO}	Sink 1mA			0.5	V
SYNCO Rise Time	t_{SYNCO_RT}	20pF load		10		ns
SYNCO Fall Time	t_{SYNCO_FT}	20pF load		10		ns
Soft Start and Tracking						
TRK Active Input Range	V_{TRK}	Internal reference tracking range	0		1.2	V
TRK Max Output Voltage	V_{TRK_MAX}			1.2		V
TRK Enable Threshold	V_{TRK_OV}		20	40	62	mV
Charge Current (Soft–Start)	I_{TRK}		–70	–50	–25	µA
Discharge Current (Fault)	I_{TRK_DIS}			6.8		mA
Soft-Start Time	t_{SS}	C_{TRK} = 0µF		2.2		ms
TRK to EAIN Offset			34		100	mV
Enable						
High Threshold	V_{EN_HI}		0.9	1	1.1	V
Low Threshold	V_{EN_LO}		0.7	0.8	0.9	V
Threshold Hysteresis	V_{EN_HYS}		100	200	300	mV
Enable Pull-Up Voltage (Floating, Unfaulted)	V_{EN_PU}	With positive-logic EN polarity		2		V
Enable Pull-Down Voltage (Floating, Faulted)	V_{EN_PD}	With negative-logic EN polarity		0		V
Source Current	I_{EN_SO}	With positive-logic EN polarity		–50		µA
Sink Current	I_{EN_SK}	With negative-logic EN polarity		50		µA

[a] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI34xx-00 evaluation board with 3 x 4in dimensions and 4 layer, 2oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[b] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control.
[c] Output current capability may be limited and other performance may vary from noted electrical characteristics when switching frequency or V_{OUT} is modified.
[d] Refer to output ripple plots.
[e] Refer to switching frequency vs. load current curves.
[f] Minimum 5V between V_{IN} – V_{OUT} must be maintained or a minimum load of 1mA required.

PI3424-00-LGIZ (5.0V_{OUT}) Electrical Characteristics (Cont.)

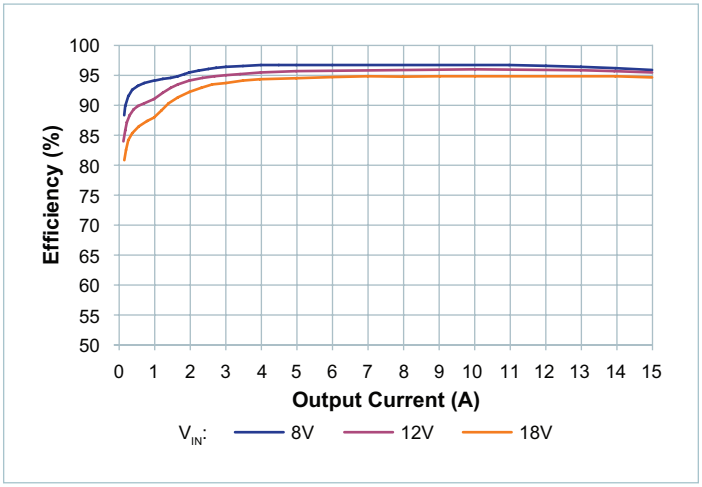


Figure 7 — *Efficiency at 25°C*

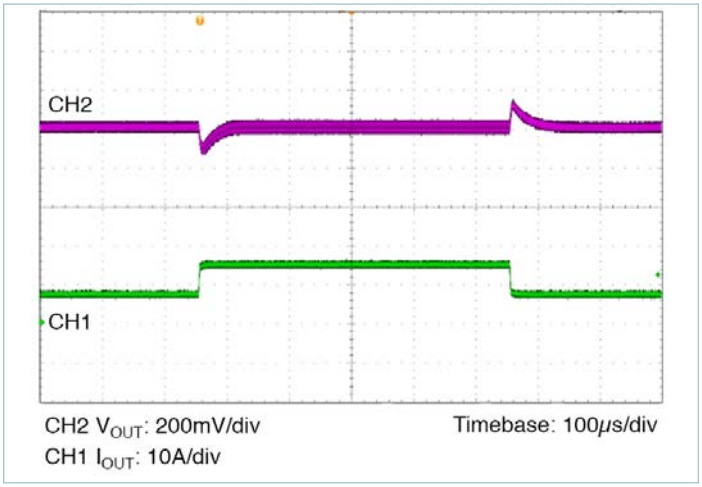


Figure 10 — *Transient response: 7.5 – 15A, at 5A/µs*

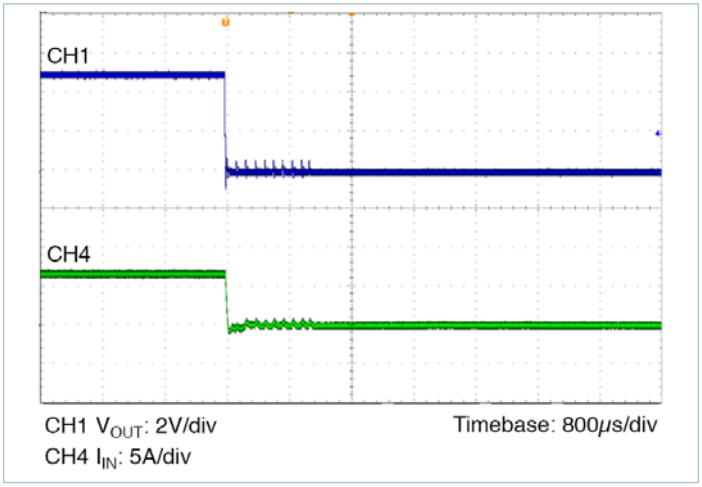


Figure 8 — *Short circuit test*

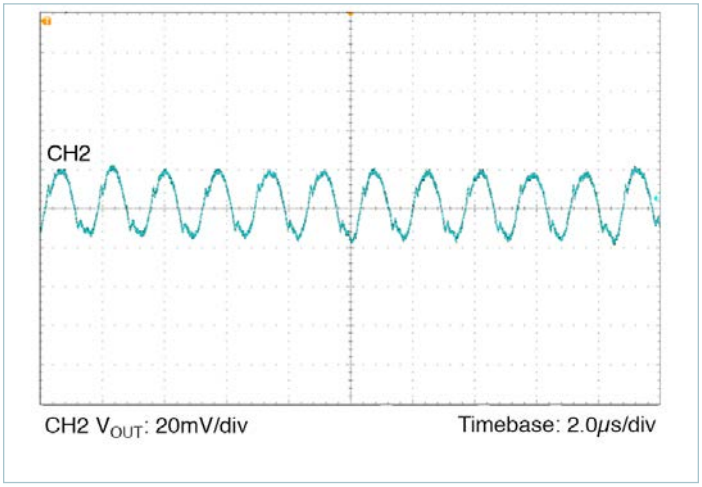


Figure 11 — *Output ripple 12V_{IN} 5.0V_{OUT} at 15A; C_{OUT} = 8 x 47µF*

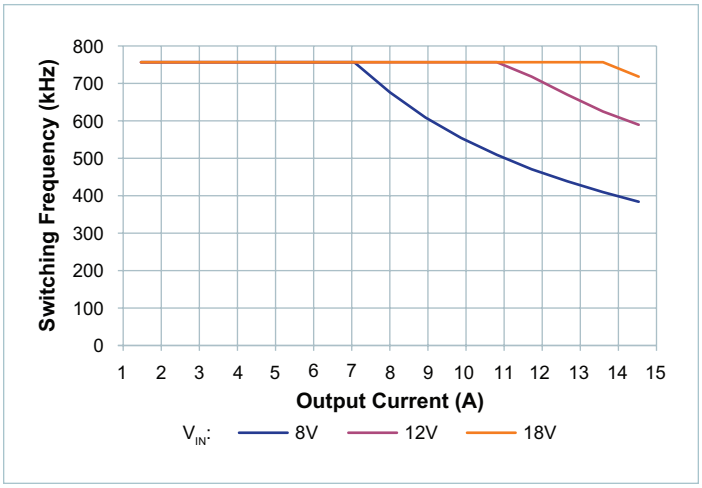


Figure 9 — *Switching frequency vs. load current*

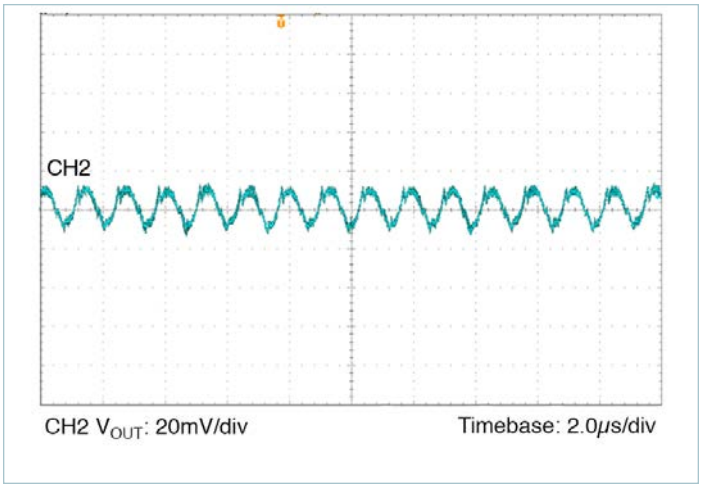


Figure 12 — *Output ripple 12V_{IN} 5.0V_{OUT} at 7.0A; C_{OUT} = 8 x 47µF*

Thermal De-Rating Curves

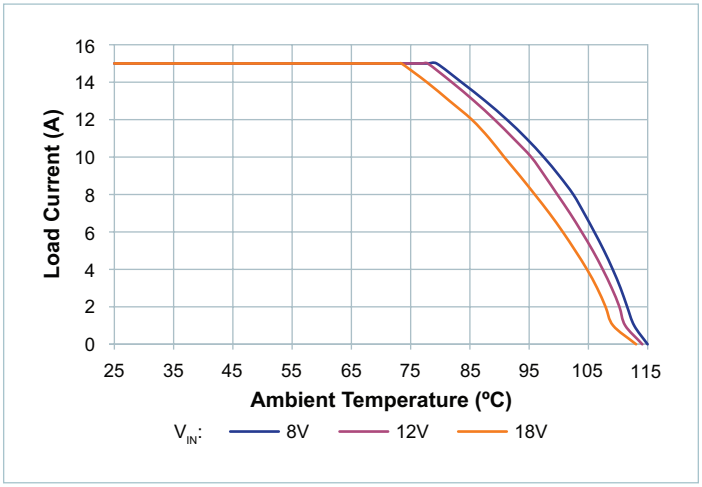


Figure 13 — *PI3423 – load current vs. ambient temperature, 0LFM*

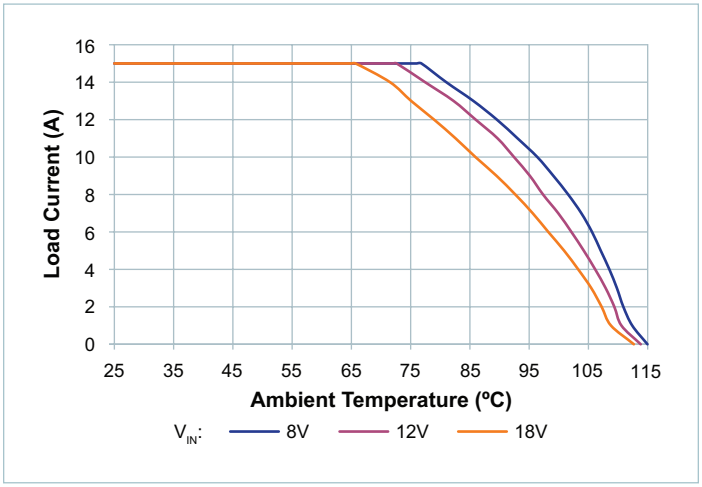


Figure 14 — *PI3424 – load current vs. ambient temperature, 0LFM*

Functional Description

The PI34xx-00 is a family of highly integrated ZVS Buck regulators. The PI34xx-00 has a set output voltage that is trimmable within a prescribed range shown in Table 1. Performance and maximum output current are characterized with a specific external power inductor (see Table 4).

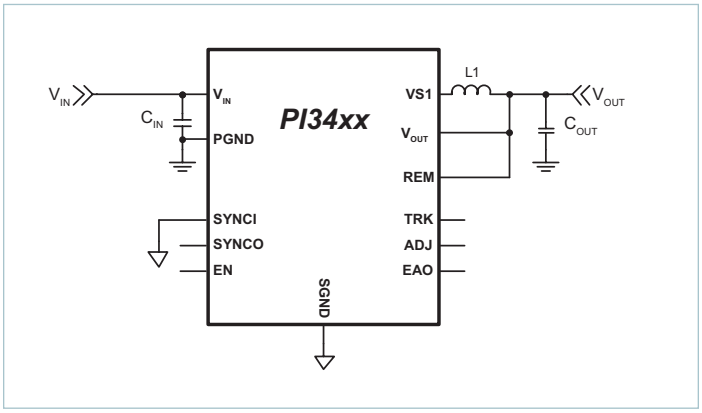


Figure 15 — *ZVS Buck with required components*

For basic operation, Figure 15 shows the connections and components required. No additional design or settings are required.

Enable (EN)

EN is the enable pin of the regulator. The EN Pin is referenced to SGND and permits the user to turn the regulator on or off. The EN polarity is a positive logic assertion. If the EN pin is left floating or asserted high, the regulator output is enabled. Pulling EN pin below $0.8V_{DC}$ with respect to SGND will disable the regulator output.

Remote Sensing

An internal 100Ω resistor is connected between REM pin and VOUT pin to provide regulation when the REM connection is broken. Referring to Figure 15, it is important to note that L1 and C_{OUT} are the output filter and the local sense point for the power supply output. As such, the REM pin should be connected at C_{OUT} as the default local sense connection unless remote sensing to compensate additional distribution losses in the system. The REM pin should not be left floating.

Switching Frequency Synchronization

The SYNCI input allows the user to synchronize the controller switching frequency by an external clock referenced to SGND. The external clock can synchronize the unit between 50 and 110% of the preset switching frequency (f_S).

The PI34xx-00 syncs to the falling edge of the applied clock providing 180° phase shift from SYNCO. This allows for the paralleling of two PI34xx-00 devices. When using the internal oscillator, the SYNCO pin provides a 5V clock that can be used to sync other regulators. Therefore, one PI34xx-00 can act as the lead regulator and have additional PI34xx-00s running in parallel and interleaved.

Soft-Start

The PI34xx-00 includes an internal soft-start capacitor to ramp the output voltage in 2ms from 0V to full output voltage. Connecting an external capacitor from the TRK pin to SGND will increase the start-up ramp period. See, "Soft Start Adjustment and Track," in the Applications Description section for more details.

Output Voltage Trim

The PI34xx-00 output voltage can be trimmed up from the preset output by connecting a resistor from ADJ pin to SGND and can be trimmed down by connecting a resistor from ADJ pin to VOUT. The Table 1 defines the voltage ranges for the PI34xx-00 family.

Device	Output Voltage	
	Set	Range
PI3423-00-LGIZ	3.3V	2.3 – 4.1V
PI3424-00-LGIZ	5.0V	3.3 – 6.5V

Table 1 — *PI34xx-00 family output voltage ranges*

Output Current Limit Protection

PI34xx-00 has two methods implemented to protect from output short or overcurrent condition.

Slow Current Limit protection: prevents the output load from sourcing current higher than the regulator's maximum rated current. If the output current exceeds the Current Limit (I_{OUT_CL}) for 1024µs, a slow current limit fault is initiated and the regulator is shut down which eliminates output current flow. After Fault Restart Delay (t_{FR_DLY}), a soft-start cycle is initiated. This restart cycle will be repeated indefinitely until the excessive load is removed.

Fast Current Limit protection: PI34xx-00 monitors the regulator inductor current pulse-by-pulse to prevent the output from supplying very high current due to sudden low impedance short (50A typical). If the regulator senses a high inductor current pulse, it will initiate a fault and stop switching until Fault Restart Delay ends and then initiate a soft-start cycle.

Input Undervoltage Lockout

If V_{IN} falls below the input Undervoltage Lockout (UVLO) threshold, the regulator will enter a low-power state and initiate a fault. The system will restart once the input voltage is reestablished and after the Fault Restart Delay.

Input Overvoltage Lockout

If V_{IN} exceeds the input Overvoltage Lockout (OVLO) threshold (V_{OVLO}), while the regulator is running, the PI34xx-00 will complete the current cycle and stop switching. The system will resume operation after the Fault Restart Delay.

Output Overvoltage Protection

The PI34xx-00 family is equipped with output Overvoltage Protection (OVP) to prevent damage to input voltage sensitive devices. If the output voltage exceeds 20% of its set regulated value, the regulator will complete the current cycle, stop switching and issue an OVP fault. The system will resume operation once the output voltage falls below the OVP threshold and after Fault Restart Delay.

Overtemperature Protection

The internal package temperature is monitored to prevent internal components from reaching their thermal maximum. If the Overtemperature Protection Threshold (OTP) is exceeded (T_{OTP}), the regulator will complete the current switching cycle, enter a low-power mode, set a fault flag, and will soft start when the internal temperature falls below Overtemperature Restart (T_{OTP_HYS}).

Parallel Operation

Paralleling modules can be used to increase the output current capability of a single power rail and reduce output voltage ripple.

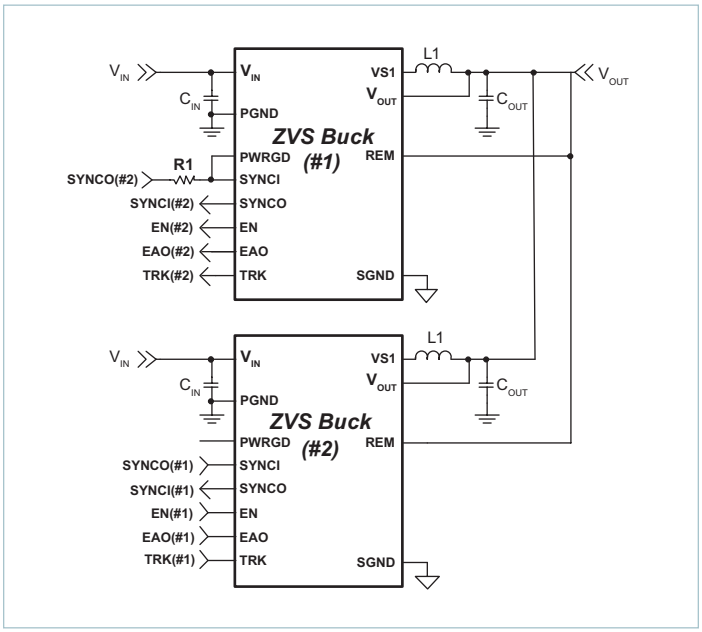


Figure 16 — *PI34xx-00 parallel operation*

By connecting the EAO pins and SGND pins of each module together the units will share the current equally. When the TRK pins of each unit are connected together, the units will track each other during soft start and all unit EN pins have to be released to allow the units to start (See Figure 16). Also, any fault event in any regulator will disable the other regulators. The two regulators will be out of phase with each other reducing output ripple (refer to Switching Frequency Synchronization).

To provide synchronization between regulators over the entire operational frequency range, the Power Good (PWRGD) pin must be connected to the lead regulator's (#1) SYNCI pin and a 2.5kΩ Resistor, R1, must be placed between SYNCO (#2) return and the lead regulator's SYNCI (#1) pin, as shown in Figure 16. In this configuration, at system soft start, the PWRGD pin pulls SYNCI low forcing the lead regulator to initialize the open-loop start-up synchronization. Once the regulators reach regulation, SYNCI is released and the system is now synchronized in a closed-loop configuration which allows the system to adjust on the fly, when any of the individual regulators begin to enter variable frequency mode in the loop.

Pulse Skip Mode (PSM)

PI34xx-00 features a PSM to achieve high efficiency at light loads. The regulators are set up to skip pulses if EAO falls below a PSM threshold. Depending on conditions and component values, this may result in single pulses or several consecutive pulses followed by skipped pulses. Skipping cycles significantly reduces gate drive power and improves light load efficiency. The regulator will leave PSM once the EAO rises above the Skip Mode threshold.

Variable-Frequency Operation

Each PI34xx-00 is preprogrammed to a base operating frequency, with respect to the power stage inductor (see Table 4), to operate at peak efficiency across line and load variations. At low-line and high-load applications, the base frequency will decrease to accommodate these extreme operating ranges. By stretching the frequency, the ZVS operation is preserved throughout the total input line voltage range therefore maintaining optimum efficiency.

Application Description

Output Voltage Trim

The PI34xx-00 family of buck regulators provides five common output voltages: 1.0, 1.8, 2.5, 3.3 and 5.0V. A post-package trim step is implemented to offset any resistor divider network errors ensuring maximum output accuracy. With a single resistor connected from the ADJ pin to SGND or REM, each device's output can be varied above or below the nominal set voltage (the PI3420-00 can only be adjusted above the set voltage of 1V).

Device	Output Voltage	
	Set	Range
PI3423-00-LGIZ	3.3V	2.3 – 4.1V
PI3424-00-LGIZ	5.0V	3.3 – 6.5V

Table 2 — *PI34xx-00 family output voltage ranges*

The remote pin (REM) should always be connected to the VOUT pin to prevent an output voltage offset. Figure 17 shows the internal feedback voltage-divider network.

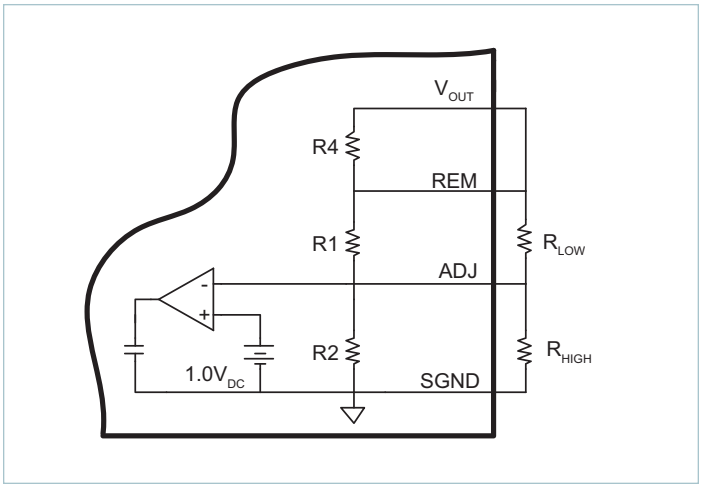


Figure 17 — *Internal resistor divider network*

R1, R2, and R4 are all internal 1.0% resistors and R_{LOW} and R_{HIGH} are external resistors for which the designer can add to modify V_{OUT} to a desired output. The internal resistor values for each regulator are listed next in Table 3.

Device	R1	R2	R4
PI3423-00-LGIZ	2.61kΩ	1.13kΩ	100Ω
PI3424-00-LGIZ	4.53kΩ	1.13kΩ	100Ω

Table 3 — *PI34xx-00 internal divider values*

By choosing an output voltage value within the ranges stated in Table 2, V_{OUT} can simply be adjusted up or down by selecting the proper R_{HIGH} or R_{LOW} value, respectively. The following equations can be used to calculate R_{HIGH} and R_{LOW} values:

$$R_{HIGH} = \frac{1}{\frac{(V_{OUT} - 1)}{R1} - \frac{1}{R2}} \qquad (1)$$

$$R_{LOW} = \frac{1}{\frac{1}{R2(V_{OUT} - 1)} - \left(\frac{1}{R1}\right)} \qquad (2)$$

If, for example, a 4.0V output is needed, the user should choose the regulator with a trim range covering 4.0V from Table 2. For this example, the PI3423 is selected (3.3V set voltage). First step would be to use Equation 1 to calculate R_{HIGH} since the required output voltage is higher than the regulator set voltage. The resistor-divider network values for the PI3423 can be found in Table 3 and are

R1 = 2.61kΩ and R2 = 1.13kΩ. Inserting these values into Equation 1, R_{HIGH} is calculated as follows:

$$3.78k = \frac{1}{\frac{(4.0 - 1)}{2.61k} - \frac{1}{1.13}}$$

Resistor R_{HIGH} should be connected as shown in Figure 17 to achieve the desired 4.0V regulator output. No external R_{LOW} resistor is need in this design example since the trim is above the regulator set voltage.

The PI3420 output voltage can only be trimmed higher than the factory 1V setting. The following Equation 3 can be used calculate R_{HIGH} values for the PI3420 regulators.

$$R_{HIGH(1V)} = \frac{1}{\frac{(V_{OUT} - 1)}{R1}} \qquad (3)$$

Soft-Start Adjust and Tracking

The TRK pin offers a means to increase the regulator's soft-start time or to track with additional regulators. The soft-start slope is controlled by an internal capacitor and a fixed charge current to provide a Soft-Start Time t_{SS} for all for all PI34xx-00 regulators. By adding an additional external capacitor to the TRK pin, the soft-start time can be increased further. The following equation can be used to calculate the proper capacitor for a desired soft-start times:

$$C_{TRK} = (t_{TRK} \bullet I_{TRK}) - 100 \times 10^{-9},$$

where, t_{TRK} is the soft-start time and I_{TRK} is a 50µA internal charge current (see Electrical Characteristics for limits).

There is typically either a proportional or direct tracking method implemented within a tracking design. For proportional tracking between several regulators at start up, simply connect all devices TRK pins together. This type of tracking will force all connected regulators to start up and reach regulation at the same time (see Figure 18 (a)).

For Direct Tracking, choose the regulator with the highest output voltage as the parent and connect the parent TRK pin to the TRK pin of the other regulators through a divider (Figure 19) with the same ratio as the child's feedback divider (see Table 3 for values).

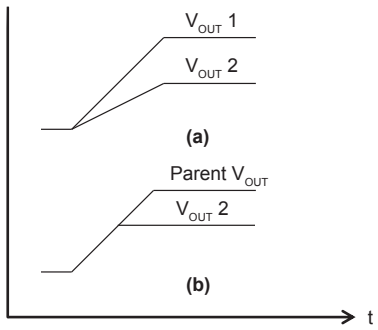


Figure 18 — *PI34xx-00 tracking methods*

All connected regulators' soft-start slopes will track with this method. Direct tracking timing is demonstrated in Figure 18 (b).

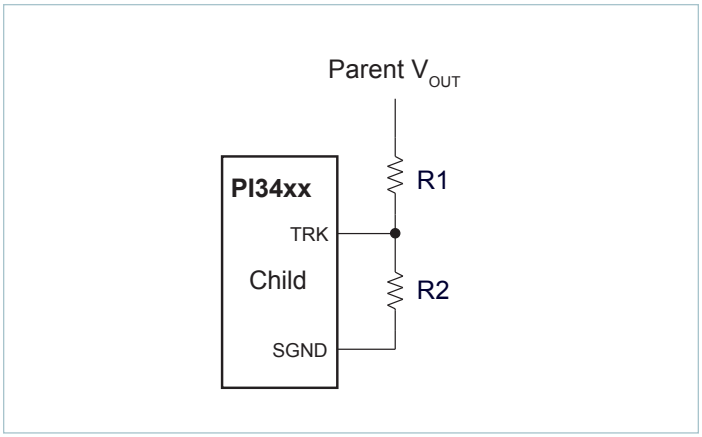


Figure 19 — *Voltage divider connections for direct tracking*

All tracking regulators should have their Enable (EN) pins connected together to work properly.

Inductor Pairing

The PI34xx-00 utilizes an external inductor from Eaton Corporation. This inductor has been optimized for maximum efficiency performance. Table 4 details the specific inductor value and part number utilized for each PI34xx-00 device.
Data sheets are available at:
www.eaton.com.

Device	Inductor (nH)	Inductor Part Number	Manufacturer
PI3423-00	150	FPV1006-150-R	Eaton
PI3424-00	150	FPV1006-150-R	Eaton

Table 4 — *PI34xx-00 inductor pairing*

Thermal De-Rating

Thermal de-rating curves are provided that are based on component temperature changes versus load current, input voltage and air flow. It is recommended to use these curves as a guideline for proper thermal de-rating. These curves represent the entire system and are inclusive to both the Vicor regulator and the external inductor. Maximum thermal operation is limited by either the MOSFETs or inductor depending upon line and load conditions.

Thermal measurements were made using a standard PI34xx-00 evaluation board which is 3 x 4 inches in area and uses 4-layer, 2oz copper. Thermal measurements were made on the three main power devices, the two internal MOSFETs and the external inductor.

Filter Considerations

The PI34xx-00 requires input bulk storage capacitance as well as low-impedance ceramic X5R input capacitors to ensure proper start up and high-frequency decoupling for the power stage. The PI34xx-00 will draw nearly all of the high-frequency current from the low-impedance ceramic capacitors when the main high-side MOSFET is conducting. During the time the high-side MOSFET is off, they are replenished from the bulk capacitor. If the input impedance is high at the switching frequency of the regulator, the bulk capacitor must supply all of the average current into the regulator, including replenishing the ceramic capacitors. This value has been chosen to be 100µF so that the PI34xx-00 can start up into a full resistive load and supply the output capacitive load with the default minimum soft-start capacitor when the input source impedance is 50Ω at 1MHz. The ESR for this capacitor should be approximately 20mΩ. The RMS ripple current in this capacitor is small, so it should not be a concern if the input recommended ceramic capacitors are used. Table 5 shows the recommended input and output capacitors to be used for the various models as well as expected transient response, RMS ripple currents per capacitor, and input and output ripple voltages. Table 6 includes the recommended input and output ceramic capacitors.

Device	V_{IN} (V)	I_{LOAD} (A)	C_{INPUT} Bulk Electrolytic	C_{INPUT} Ceramic X5R	C_{OUTPUT} Ceramic X5R	C_{INPUT} Ripple Current (I_{RMS})	C_{OUTPUT} Ripple Current (I_{RMS})	Input Ripple (mV_{P-P})	Output Ripple (mV_{P-P})	Output Ripple (mV_{PK})	Recovery Time (µs)	Load Step (A) [Slew/µs]
PI3423	12	15	100µF 50V	6 x 22µF	8 x 100µF 2 x 1µF 1 x 0.1µF	1.20	1.15	179	26	±73	70	7.5 [5A/µs]
		7.5						97	17			
PI3424	12	15	100µF 50V	6 x 22µF	8 x 100µF 2 x 1µF 1 x 0.1µF	1.29	1.13	209	34	±98	60	7.5 [5A/µs]
		7.5						98	24.8			

Table 5 — *Recommended input and output capacitance*

Murata Part Number	Description
GRM188R71C105KA12D	1µF 16V 0603 X7R
GRM319R71H104KA01D	0.1µF 50V 1206 X7R
GRM31CR60J107ME39L	100µF 6.3V 1206 X5R
GRM31CR61A476ME15L	47µF 10V 1206 X5R
GRM31CR61E226KE15L	22µF 25V 1206 X5R

Table 5 — *Capacitor manufacturer part numbers*

Layout Guidelines

To achieve maximum efficiency and low-noise performance from a PI34xx-00 design, layout considerations are necessary. Reducing trace resistance and minimizing high-current loop returns along with proper component placement will contribute to optimal performance.

A typical buck regulator circuit is shown in Figure 20. The potential areas of high parasitic inductance and resistance are the circuit return paths, shown as LR below.

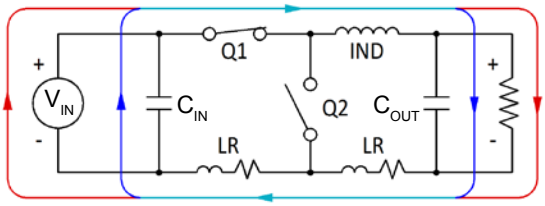


Figure 20 — *Typical buck regulator*

The path between the C_{OUT} and C_{IN} capacitors is of particular importance since the AC currents are flowing through both of them when Q1 is turned on.

Figure 21, schematically, shows the reduced trace length between input and output capacitors. The shorter path lessens the effects that copper trace parasitics can have on the PI34xx-00 performance.

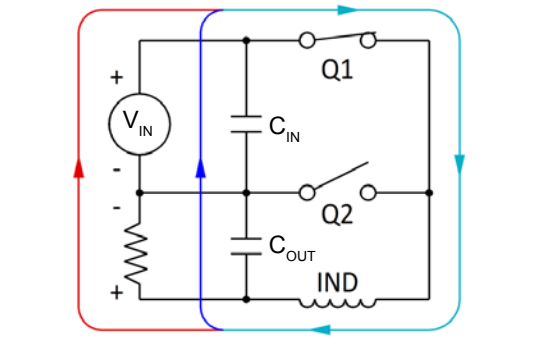


Figure 21 — *Current flow: Q1 closed*

When Q1 is on and Q2 is off, the majority of C_{IN}'s current is used to satisfy the output load and to recharge the C_{OUT} capacitors. When Q1 is off and Q2 is on, the load current is supplied by the inductor and the C_{OUT} capacitor as shown in Figure 22. During this period C_{IN} is also being recharged by the V_{IN}. Minimizing C_{IN} loop inductance is important to reduce peak voltage excursions when Q1 turns off. Also, the difference in area between the C_{IN} loop and C_{OUT} loop is vital to minimize switching and GND noise.

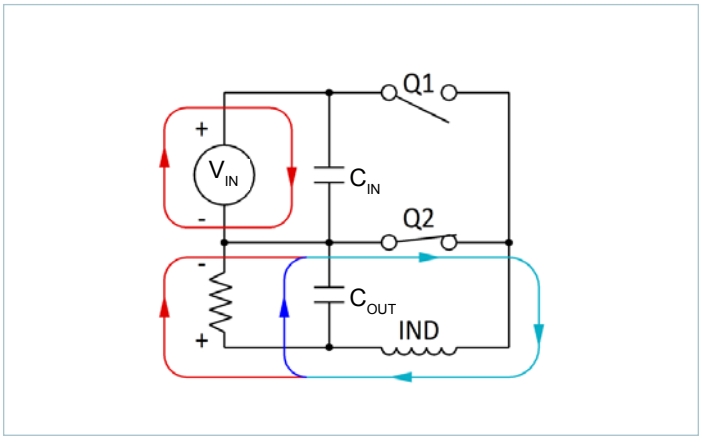


Figure 22 — *Current flow: Q2 closed*

The recommended component placement, shown in Figure 23, illustrates the tight path between C_{IN} and C_{OUT} (and V_{IN} and V_{OUT}) for the high AC return current. This optimized layout is used on the PI34xx-00 evaluation board.

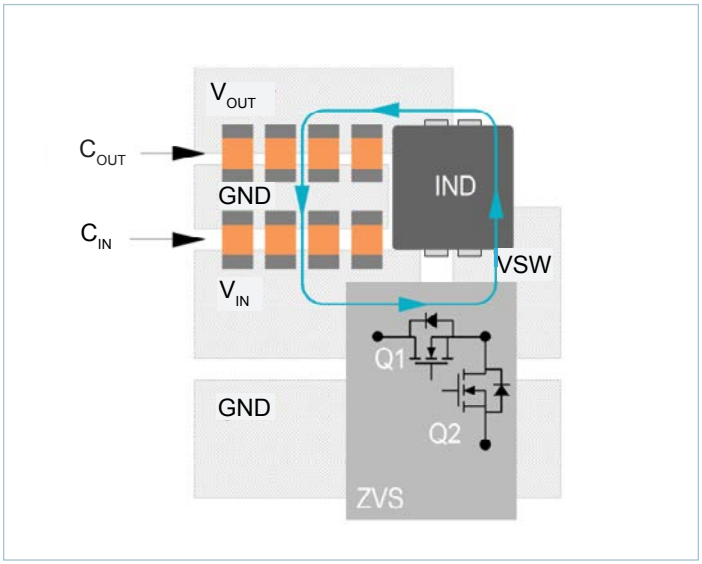
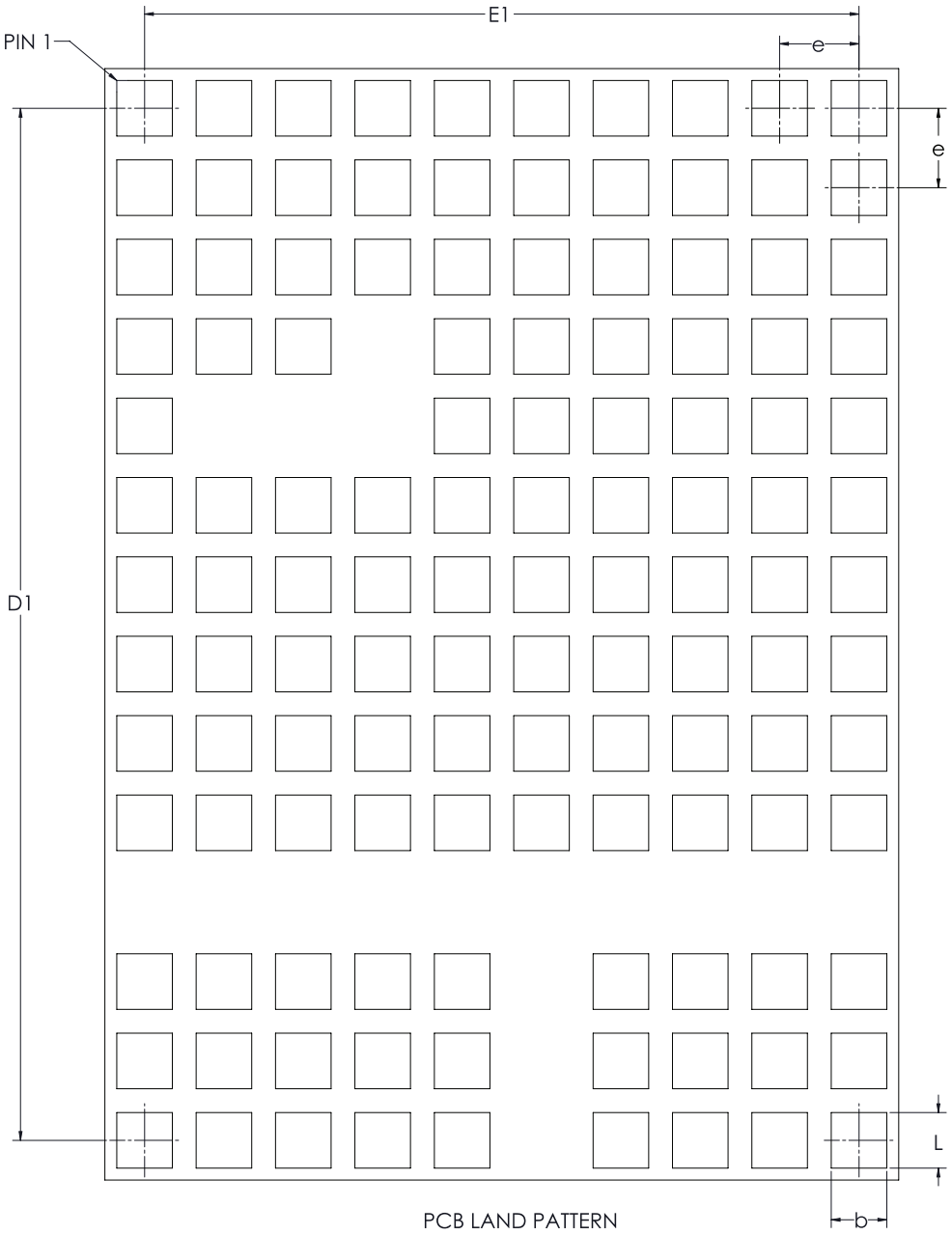


Figure 23 — *Recommended component placement and metal routing*

Recommended PCB Footprint and Stencil



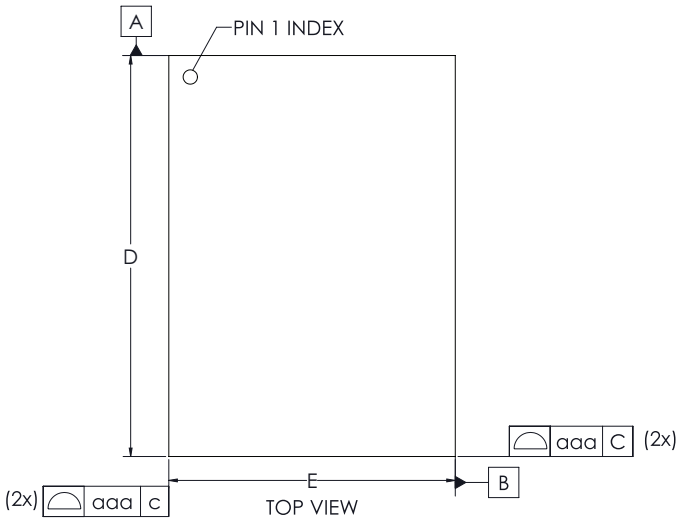
PCB LAND PATTERN

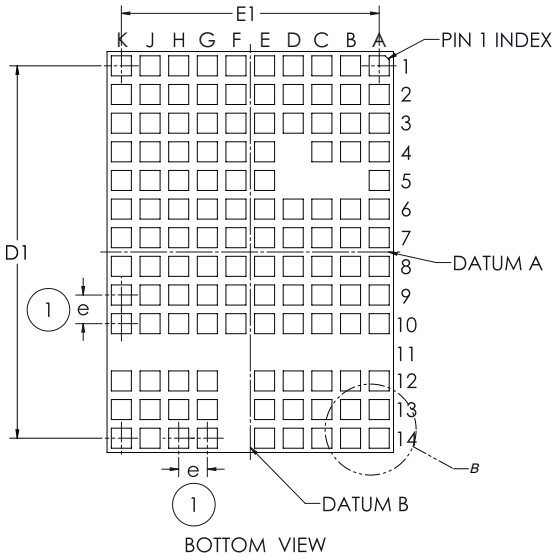
PI34xx-00

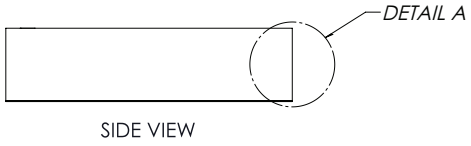
DIMENSIONAL REFERENCES			
REF.	MIN.	NOM.	MAX.
b	0.50	0.55	0.60
D1		13.00 BSC	
E1		9.00 BSC	
e		1.00 BSC	
L	.50	.55	.60

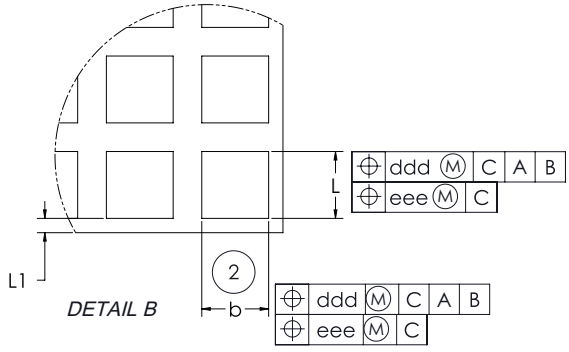
Recommended receiving footprint for PI34xx-00 10 x 14mm package. All pads should have a final copper size of 0.55 x 0.55mm, whether they are solder-mask defined or copper defined, on a 1 x 1mm grid. All stencil openings are 0.45mm when using either a 5 or 6mil stencil.

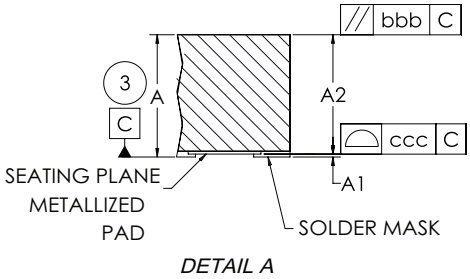
Package Drawings











10 x 14mm SIP			
DIMENSIONAL REFERENCES			
REF.	MIN.	NOM.	MAX.
A	2.49	2.56	2.63
A1	--	--	0.04
A2	--	--	2.59
b	0.50	0.55	0.60
L	0.50	0.55	0.60
D		14.00 BSC	
E		10.00 BSC	
D1		13.00 BSC	
E1		9.00 BSC	
e		1.00 BSC	
L1	0.175	0.225	0.250

NOTES:
1. 'e' REPRESENTS THE BASIC TERMINAL PITCH. SPECIFIES THE TRUE GEOMETRIC POSITION OF THE TERMINAL AXIS.
2. DIMENSION 'b' APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.00mm AND 0.25mm FROM TERMINAL TIP.
3. DIMENSION 'A' INCLUDES PACKAGE WARPAGE
4. EXPOSED METALLIZED PADS ARE CU PADS WITH SURFACE FINISH PROTECTION.
5. ALL DIMENSIONS ARE IN MM UNLESS OTHERWISE SPECIFIED.
6. RoHS COMPLIANT PER CST-0001 LATEST REVISION.

DIMENSIONAL REFERENCES	
REF.	TOLERANCE OF FORM AND POSITION
aaa	0.10
bbb	0.10
ccc	0.08
ddd	0.10
eee	0.08

Revision History

Revision	Date	Description	Page Number(s)
1.0	02/13	Last release in old format	n/a
1.1	08/03/15	Reformatted in new template	n/a
1.2	09/03/15	Inductor pairing table updates	6, 7 & 25
1.3	12/21/15	Clarifications made in Enable Pin Conditions	7, 8, 11, 14, 17 & 28
1.4	02/03/20	Formatting changes Changed PGD pin name to PWRGD Removed continuous output current range min Corrected UVLO stop hysteresis, OVLO stop threshold, OVLO start hysteresis Updated sink current Added TRK to EAIN offset spec, revised soft-start charge current, TRK enable threshold Updated input quiescent current enabled Updated output voltage total regulation Updated mechanical drawings	All 3, 4, 5, 7 7, 10, 13, 16, 19 8 8, 11, 14, 17, 20 10 10, 16 28, 29
1.5	02/26/20	Added CDM ESD rating	3
1.6	05/14/20	Corrected REM absolute maximum rating	3
1.7	08/11/20	Updated terminology	25, 26
1.8	12/31/20	Removed end-of-life part numbers (for PI3420-00, PI3421-00 and PI3422-00 data, see separate document) Revised PI3424-00 switching frequency vs. load current plot	 1 – 3 12
1.9	01/04/21	Revised switching frequency typical specification	11
2.0	02/24/21	Revised UVLO start threshold Added SYNCI input impedance specification	7, 10 8, 11
2.1	09/01/21	Corrected figure 1 plot	9
2.2	01/14/22	Corrections to figures 1, 2, 4, 7, 8, 10 removed irrelevant figures	9, 12 13

Note: page added in Rev 1.4, pages removed in Rev 1.8.

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