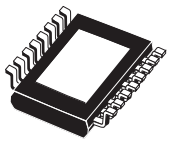
STAP08DP05

Low voltage 8-bit constant current LED sink driver with output error detection for automotive applications

Datasheet - production data



TSSOP16
(Exposed pad)

Features

- AECQ100 qualification
- Low voltage power supply down to 3 V
- 8 constant current output channels
- Adjustable output current through external resistor
- Short and open output error detection
- Serial data IN/parallel data OUT
- Able to drive 3.3 V microcontroller
- Output current: 5-100 mA
- 30 MHz clock frequency
- Available in high thermal efficiency TSSOP exposed pad
- ESD protection 2.5 kV HBM

Applications

- Dashboard and infotainment backlighting
- Exterior/interior lighting
- DTRLs

Description

The STAP08DP05 is a monolithic, low voltage, low current power 8-bit shift register designed for LED panel displays. The STAP08DP05 contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. In the output stage, eight regulated current sources are designed to provide 5-100 mA constant current to drive the LEDs.

The detection circuit checks 3 different conditions that can occur on the output line: short to GND, short to V_O or open line. The data detection results are loaded in the shift register and shifted out via the serial line output.

STAP08DP05 detection functionality is implemented without increasing the pin number. Through a secondary function of the output enable and latch pin (DM1 and DM2 respectively), a dedicated logic sequence allows the device to enter or leave detection mode. Through an external resistor, users can adjust the output current of the STAP08DP05, thus controlling the light intensity of the LEDs. In addition, the user can adjust the intensity of the brightness of the LEDs from 0% to 100% through the $\overline{OE}$/DM2 pin.

The STAP08DP05 guarantees a 20 V output driving capability, allowing users to connect more LEDs in series. The high clock frequency, 30 MHz, also satisfies the system requirement of high volume data transmission. The 3.3 V of voltage supply is very useful for applications that interface any microcontroller from 3.3 V. Compared with a standard TSSOP package, the TSSOP exposed pad increases the capability of heat dissipation by a factor of 2.5.

Table 1. Device summary

Order code	Package	Packing
STAP08DP5XTTR	TSSOP16 exposed-pad (Tape and reel)	2500 parts per reel

Contents

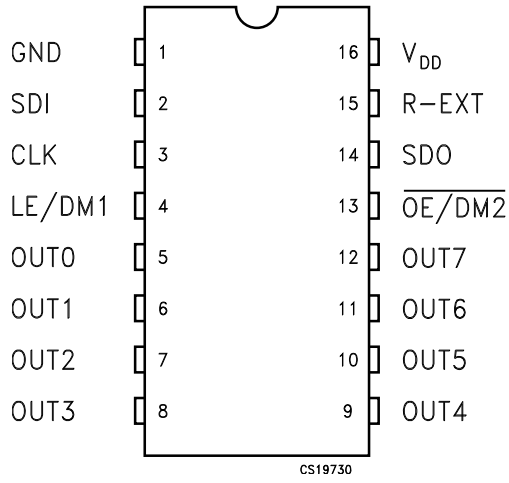
1 Summary description

Table 2. Typical current accuracy

Output voltage	Current accuracy		Output current
	Between bits	Between ICs	
≥1.3 V	±1.5%	±6%	20 to 100 mA

1.1 Pin connections and description

Figure 1. Pin connections



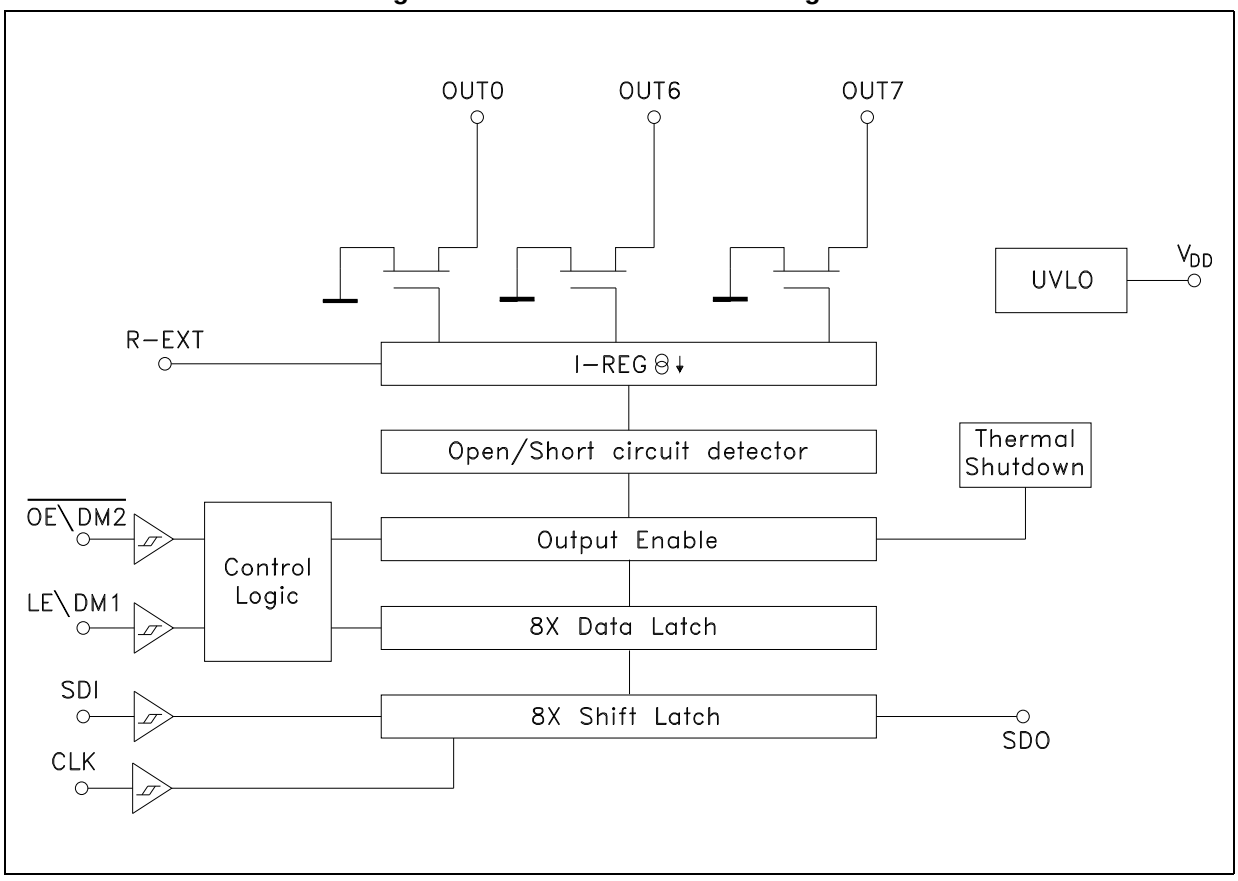
Note: The exposed pad is electrically connected to a metal layer electrically isolated or connected to ground.

Table 3. Pin description

Pin n°	Symbol	Name and function
1	GND	Ground terminal
2	SDI	Serial data input terminal
3	CLK	Clock input terminal
4	LE/DM1	Latch input terminal
5-12	OUT 0-7	Output terminal
13	$\overline{OE}$/DM2	Output enable input terminal (active low)
14	SDO	Serial data out terminal
15	R-EXT	Constant current programming
16	V_{DD}	5 V supply voltage terminal

2 Block diagram

Figure 2. Normal mode - block diagram



3 Maximum rating

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage I_{GND}	0 to 7	V
V_O	Output voltage	-0.5 to 20	V
I_O	Output current	100	mA
I_{GND}	GND terminal current	800	mA
f_{CLK}	Clock frequency	50	MHz
T_{OPR}	Operating temperature range	-40 to +150	°C
T_{STG}	Storage temperature range	-55 to +150	°C

3.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Value (1)	Unit
R_{thJA}	Thermal resistance junction-ambient	37.5	°C/W

1. The exposed pad should be soldered to the PCB in order to derive the thermal benefits (according to Jedec 51-7).

3.3 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage		3.0	-	5.5	V
V_O	Output voltage			-	20	V
I_O	Output current	OUTn	5	-	100	mA
I_{OH}	Output current	SERIAL-OUT		-	+1	mA
I_{OL}	Output current	SERIAL-OUT		-	-1	mA
V_{IH}	Input voltage		0.7 V_{DD}	-	V_{DD}+0.3	V
V_{IL}	Input voltage		-0.3	-	0.3V_{DD}	V
t_{wLAT}	LE/DM1 pulse width	V_{DD} = 3.0 to 5.0 V	20	-		ns
t_{wCLK}	CLK pulse width		20	-		ns
t_{wEN}	$\overline{OE}$/DM2 pulse width		200	-		ns
$t_{SETUP(D)}$	Setup time for DATA		7	-		ns
$t_{HOLD(D)}$	Hold time for DATA		4	-		ns
$t_{SETUP(L)}$	Setup time for LATCH		15	-		ns
f_{CLK}	Clock frequency	Cascade operation (1)		-	30	MHz

1. If the device is connected in cascade, it may not be possible to achieve the maximum data transfer. Please consider the timings carefully.

4 Electrical characteristics

V_{DD} = 5 V, T_j = -40 °C to 125 °C, unless otherwise specified.

Table 7. Electrical characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{IH}	Input voltage high level		0.7•VDD		VDD	V
V_{IL}	Input voltage low level		GND		0.3•VDD	
V_{OL}	Serial data output voltage (SDO)	I_{OL} = + 1 mA		0.03	0.4	
V_{OH}		I_{OH} = - 1 mA	VDD-0.4			
I_{OH}	Output leakage current	Vo =19 V, Outn = OFF		0.5	2	µA
ΔI_{OL1}	Current accuracy channel-to-channel (1) (2)	VDD = 3.3 V, V_O = 0.3 V Rext = 3.9 kΩ			8	%
ΔI_{OL2}		VDD = 3.3 V, V_O = 0.4 V Rext = 980 Ω			4	
ΔI_{OL3}		VDD = 3.3 V, V_O = 1.3 V Rext = 200 Ω			4	
ΔI_{OL2}	Current accuracy device-to-device (1)	VDD = 3.3 V, V_O = 0.4 V Rext = 980 Ω			6	
ΔI_{OL3}		VDD = 3.3 V, V_O = 1.3 V Rext = 200 Ω			6	
R_{IN}(up)	Pull-up resistor for OE pin		150	300	600	kΩ
R_{IN}(down)	Pull-down resistor for LE pin		100	200	400	
IDD(OFF1)	Supply current (OFF)	R ext = 980 Ω, LE = I_{ow}, OUT0 to OUT7 = OFF		4	6.5	mA
IDD(OFF2)		Rext = 200 Ω, LE = I_{ow}, OUT0 to OUT15 = OFF		11	16	
IDD(ON1)	Supply current (ON)	Rext = 980 Ω, LE = I_{ow}, OUT0 to OUT15 = ON		4.5	6.5	
IDD(ON2)		Rext = 200 Ω, LE = I_{ow}, OUT0 to OUT15 = ON		12	16	
Tsd	Thermal shutdown (3)			170		°C

1. Test performed with all outputs turned on, but only one output loaded at a time.
2. ΔIOL+ = ((IOLmax - IOLmean)/ IOLmean)*100, ΔIOL- = ((IOLmin - IOLmean)/ IOLmean)*100, where IOLmean = (IOLout1+IOLout2+…+IOLout16) / 16.
3. Not tested, guaranteed by design.

5 Switching characteristics

V_{DD} = 5 V, T_j = 25 °C, unless otherwise specified.

Table 8. Switching characteristics(1)(2)

Symbol	Parameter		Test conditions		Min	Typ	Max	Unit
f_{clk}	Clock frequency		Cascade operation				30	MHz
tPLH1	CLK-OUTn LE\DM1 = H OE\DM2 = L	Propagation delay time (“L” to “H”)	VIH = VDD VIL = GND CL = 10 pF Io = 20 mA VL = 3 V REXT = 1 KΩ RL = 60 Ω	VDD = 3.3 V		36	50	ns
				VDD = 5 V		19	25	
tPLH2	LE\DM1-OUTn OE\DM2 = L			VDD = 3.3 V		38	50	ns
				VDD = 5 V		21	30	
tPLH3	OE\DM2-OUTn LE\DM1 = H			VDD = 3.3 V		42	55	ns
				VDD = 5 V		23	30	
tPLH	CLK - SDO			VDD = 3.3 V		22	30	ns
				VDD = 5 V		18	25	
tPHL1	CLK-OUTn LE\DM1 = H OE\DM2 = L	Propagation delay time (“H” to “L”)		VDD = 3.3 V		9	12	ns
				VDD = 5 V		5	7	
tPHL2	LE\DM1-OUTn OE\DM2 = L			VDD = 3.3 V		4	6	ns
				VDD = 5 V		3	5	
tPHL3	OE\DM2-OUTn LE\DM1 = H			VDD = 3.3 V		6	8	ns
				VDD = 5 V		3	5	
tPHL	CLK - SDO			VDD = 3.3 V		25	33	ns
				VDD = 5 V		20	26	
t_{ON}	Output rise time 10~90% of voltage waveform			VDD = 3.3 V		30	40	ns
				VDD = 5 V		15	20	
t_{OFF}	Output fall time 90~10% of voltage waveform			VDD = 3.3 V		7	10	ns
				VDD = 5 V		6	8	
tr	CLK rise time (3)						5	µs
tf	CLK fall time (3)						5	

1. All table limits are guaranteed by design.
2. Not tested in production.
3. If devices are connected in cascade and tr or tf is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

6 Equivalent circuit and outputs

Figure 3. $\overline{\text{OE}}$/DM2 terminal

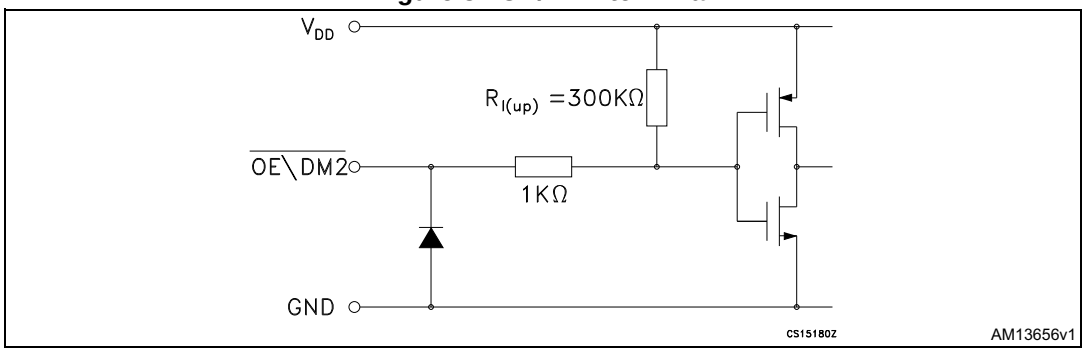


Figure 4. LE/DM1 terminal

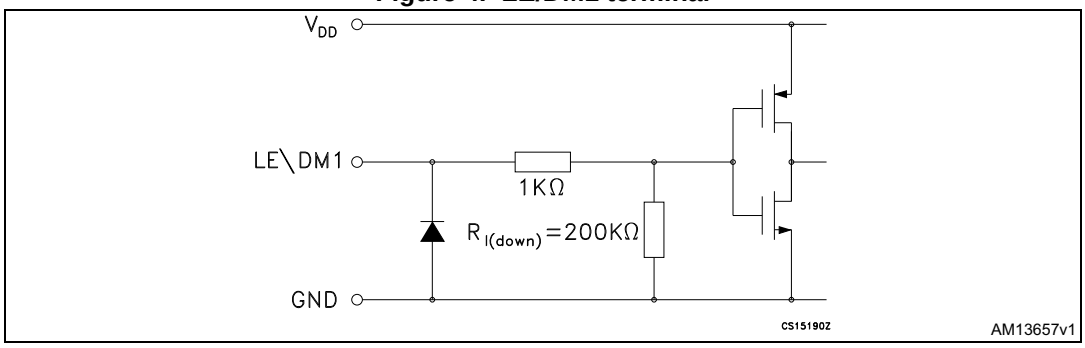


Figure 5. CLK, SDI terminal

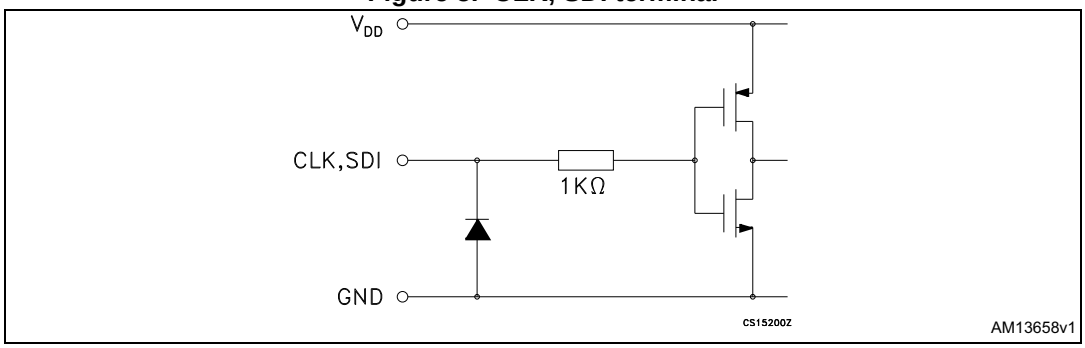
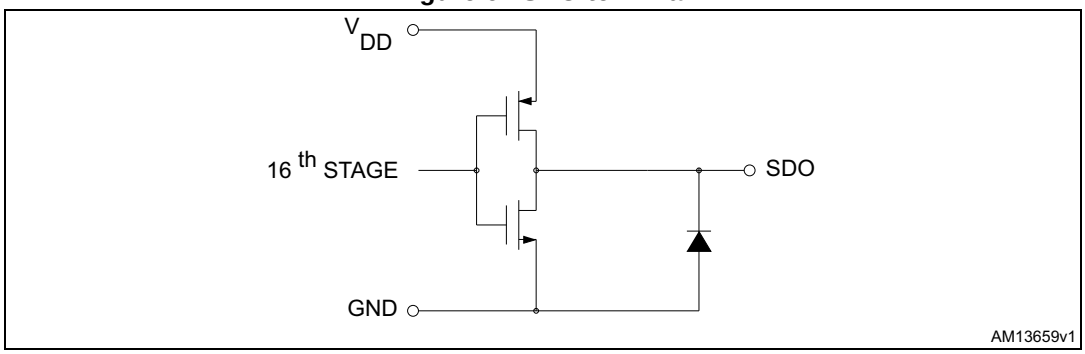


Figure 6. SDO terminal



7 Truth table and timing diagrams

7.1 Truth table

Table 9. Truth table

Clock	LE/DM1	$\overline{OE/DM2}$	SDI	$\overline{OUT0}$ ..... $\overline{OUT0}$ ..... $\overline{OUT7}$	SDO
↑	H	L	Dn	Dn ..... Dn -5 ..... Dn -7	Dn -7
↑	L	L	Dn + 1	No change	Dn -7
↑	H	L	Dn + 2	$\overline{Dn+2}$ ..... $\overline{Dn-3}$ ..... $\overline{Dn-5}$	Dn -5
↓	X	L	Dn + 3	$\overline{Dn+2}$ ..... $\overline{Dn-3}$ ..... $\overline{Dn-5}$	Dn -5
↓	X	H	Dn + 3	OFF	Dn -5

Note: OUT0 to OUT7 = ON when Dn = H; OUT0 to OUT7 = OFF when Dn = L.

7.2 Timing diagrams

Figure 7. Timing diagram - normal mode

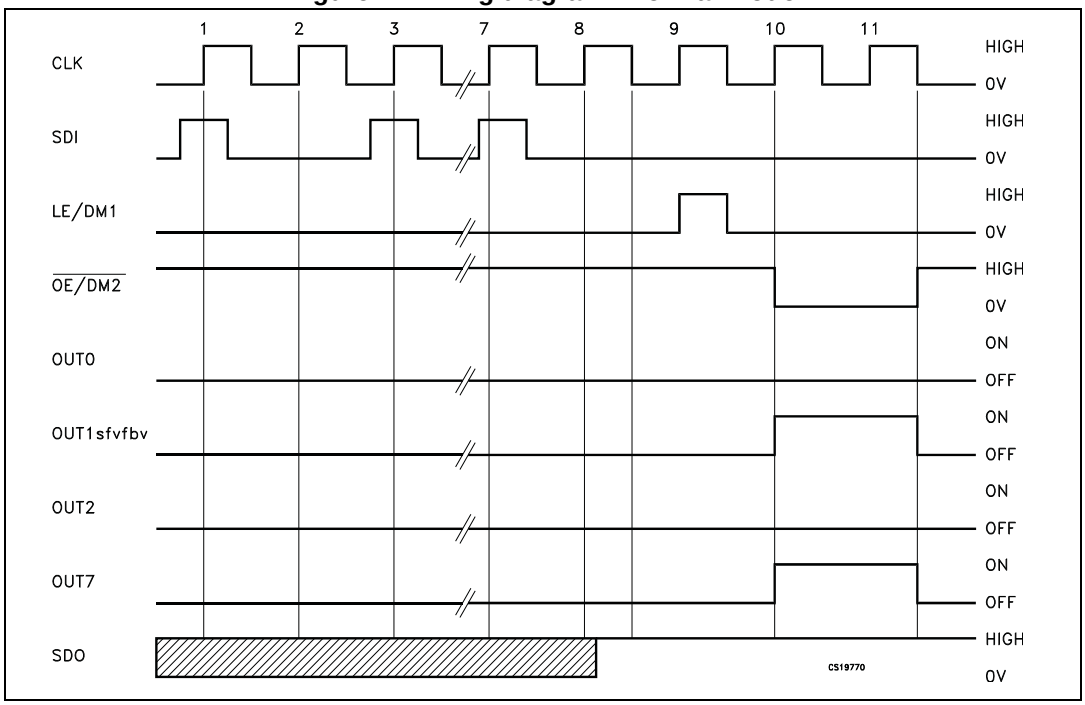


Figure 8. Clock, serial-in, serial-out

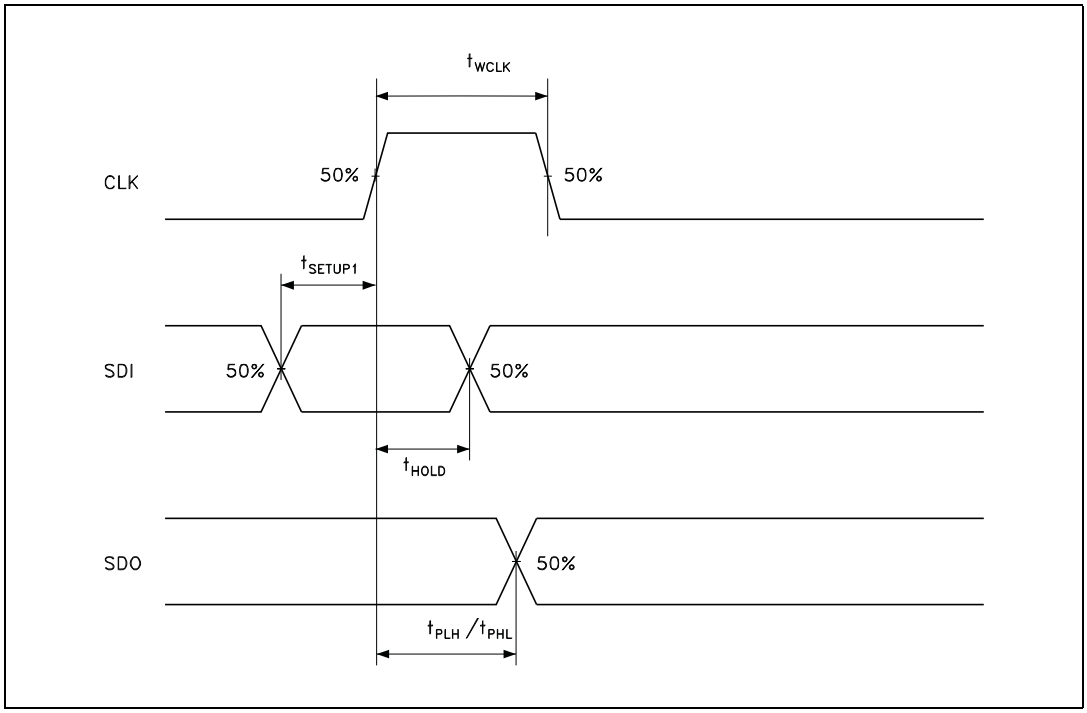


Figure 9. Clock, serial-in, latch, enable, outputs

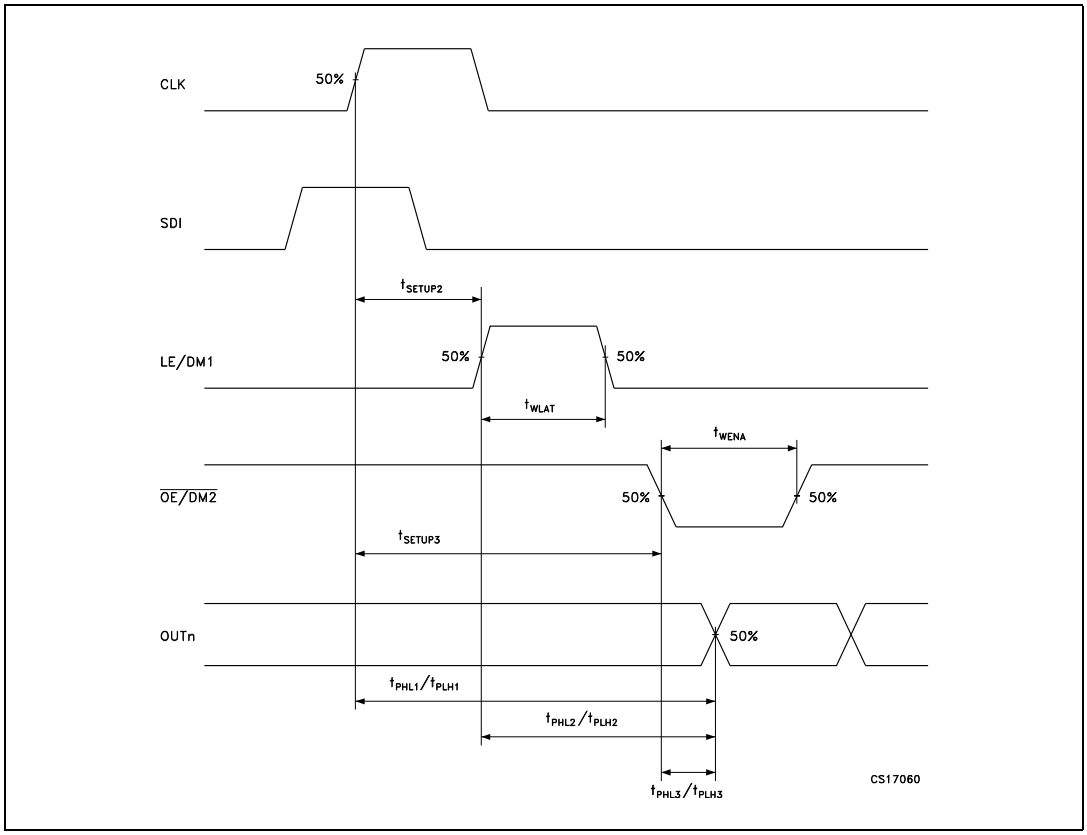
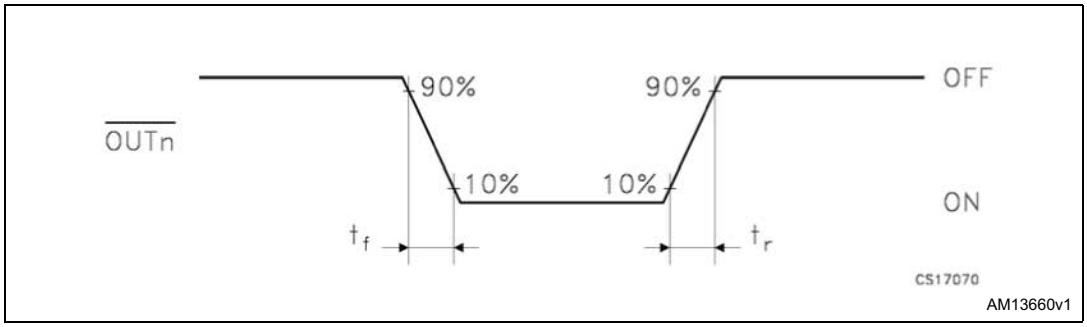


Figure 10. Outputs



8 Typical characteristics

Figure 11. Output current - R_{EXT} resistor

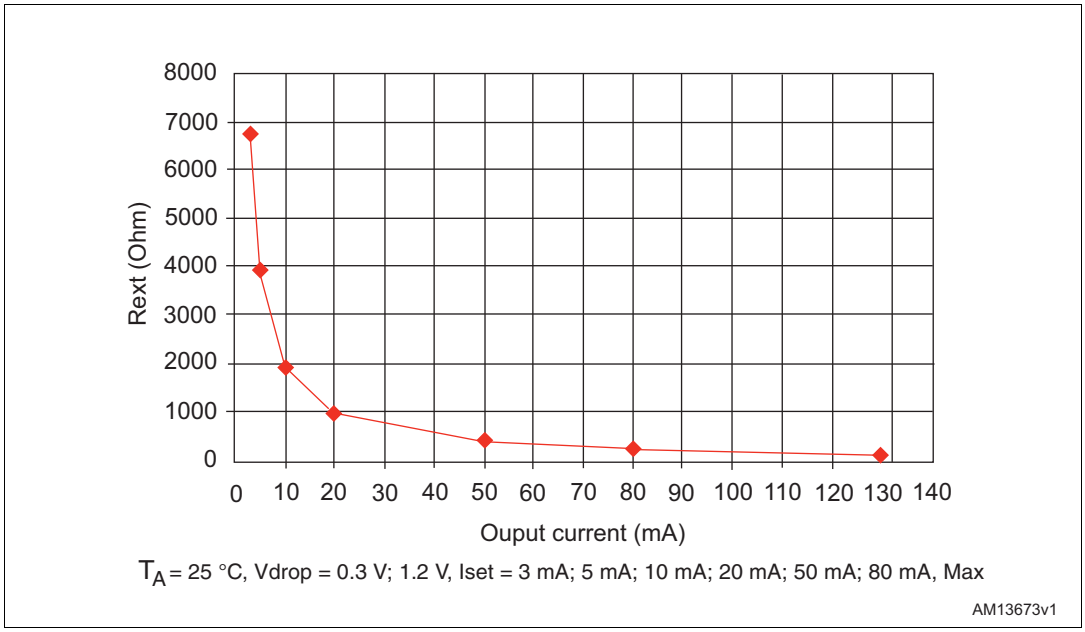


Table 10. Output current - R_{EXT} resistor, T_A = 25 °C

Parameter	Value						
Output current (mA)	3	5	10	20	50	80	130
Rext (Ω)	6740	3930	1913	963	386	241	124

Note: Maximum output current setting was 130 mA applying Rext = 124 Ω.

Figure 12. I_{SET} vs. drop-out voltage (V_{DROP} @ 25 °C)

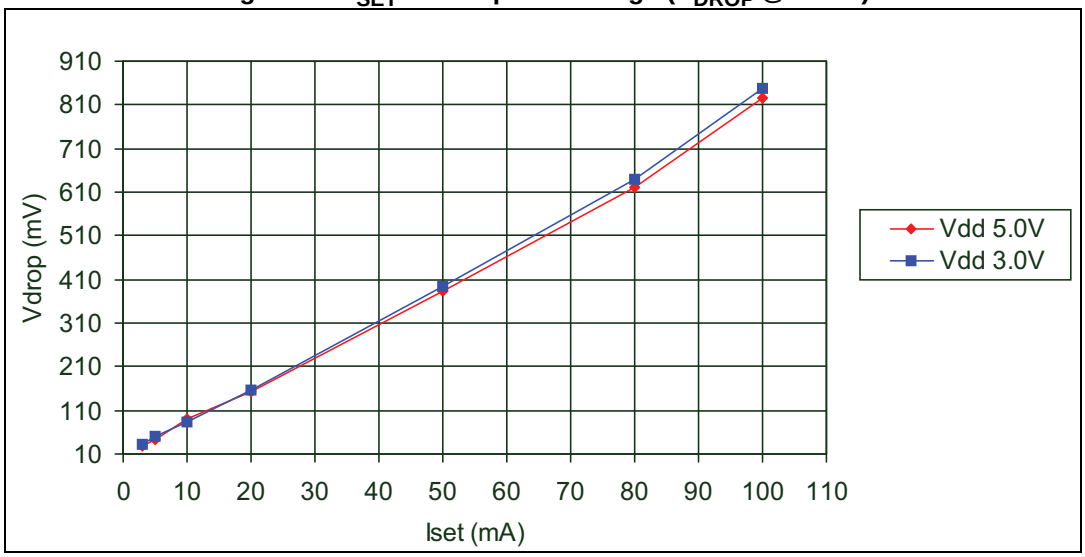
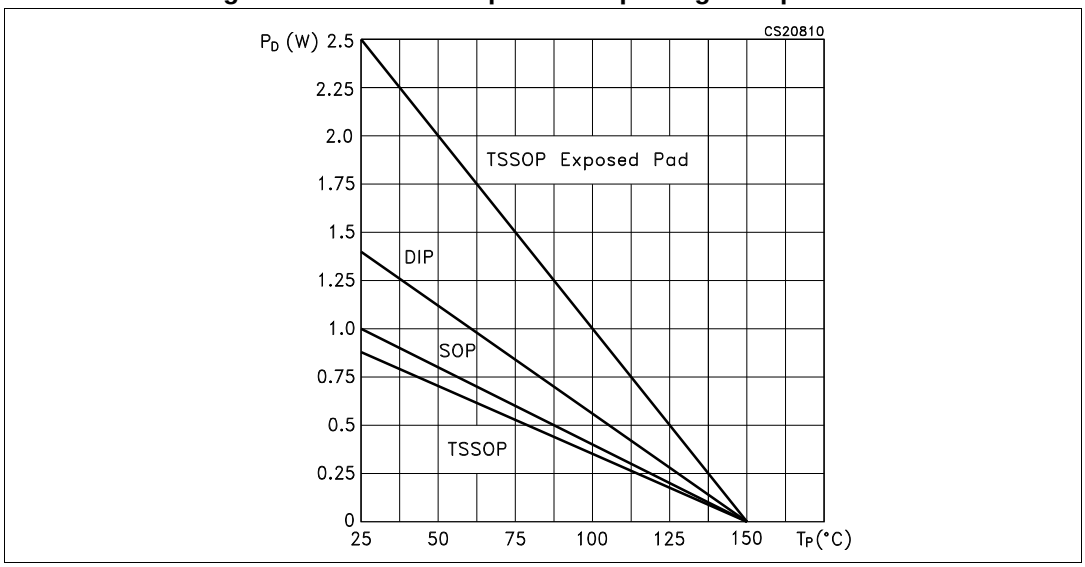


Table 11. I_{SET} vs. drop-out voltage (V_{DROP} @ 25 °C)

Vdd (V)	I set (mA)	Rext (Ω)	Vdrop min (mV)	Vdrop max (mV)	Vdrop AVG (mV)
3	3	6470	30.6	31.2	30.93
	5	3930	46.5	52.9	48.63
	10	1910	80.9	100	82.26
	20	963	150	161	157
	50	386	392	396	394.3
	80	241	636	646	640.3
	100	192	846	850	848
5	3	6470	25.6	29	26.96
	5	3930	40.8	41.7	41.16
	10	1910	80.1	105	89.2
	20	963	153	154	154
	50	386	379	386	382
	80	241	618	626	621
	100	192	825	830	827

Figure 13. Power dissipation vs. package temperature



Note: The exposed pad should be soldered to the PCB in order to derive the thermal benefits (according to Jedec 51-7).

9 Test circuit

Figure 14. DC characteristics

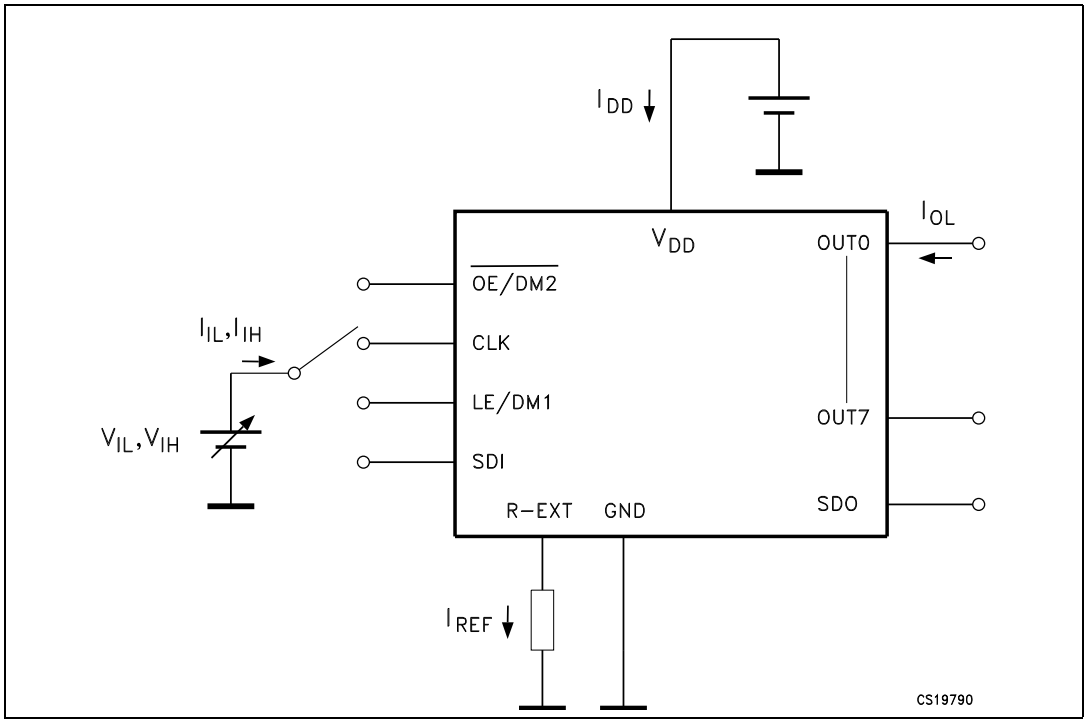


Figure 15. AC characteristics

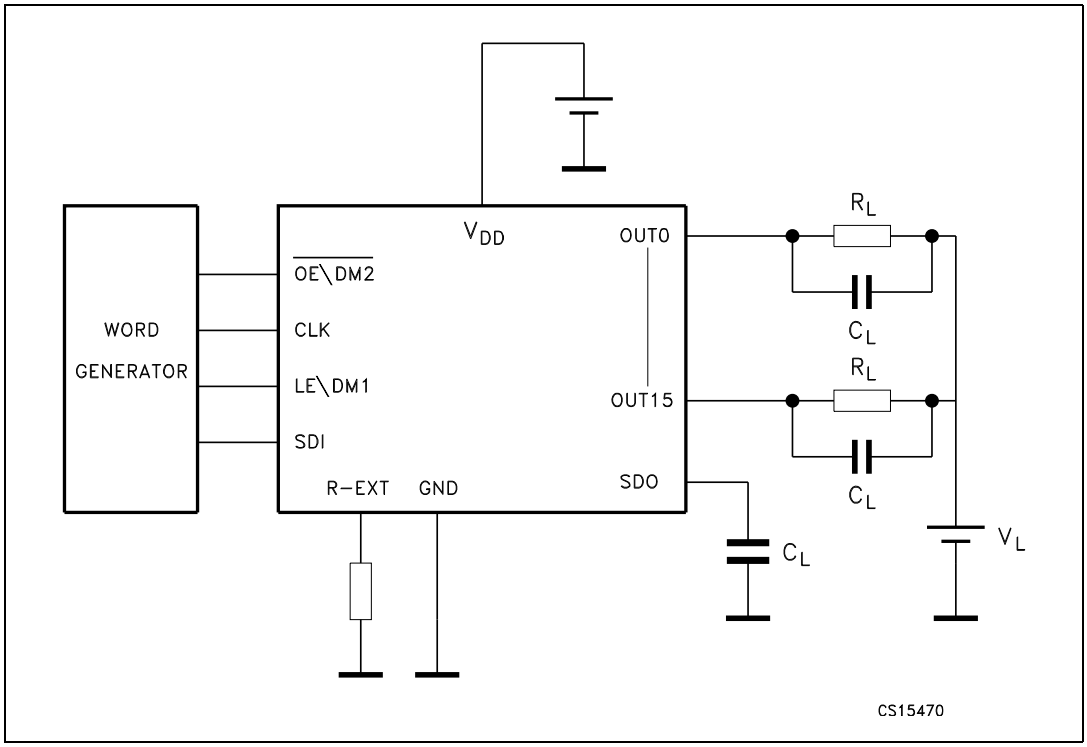
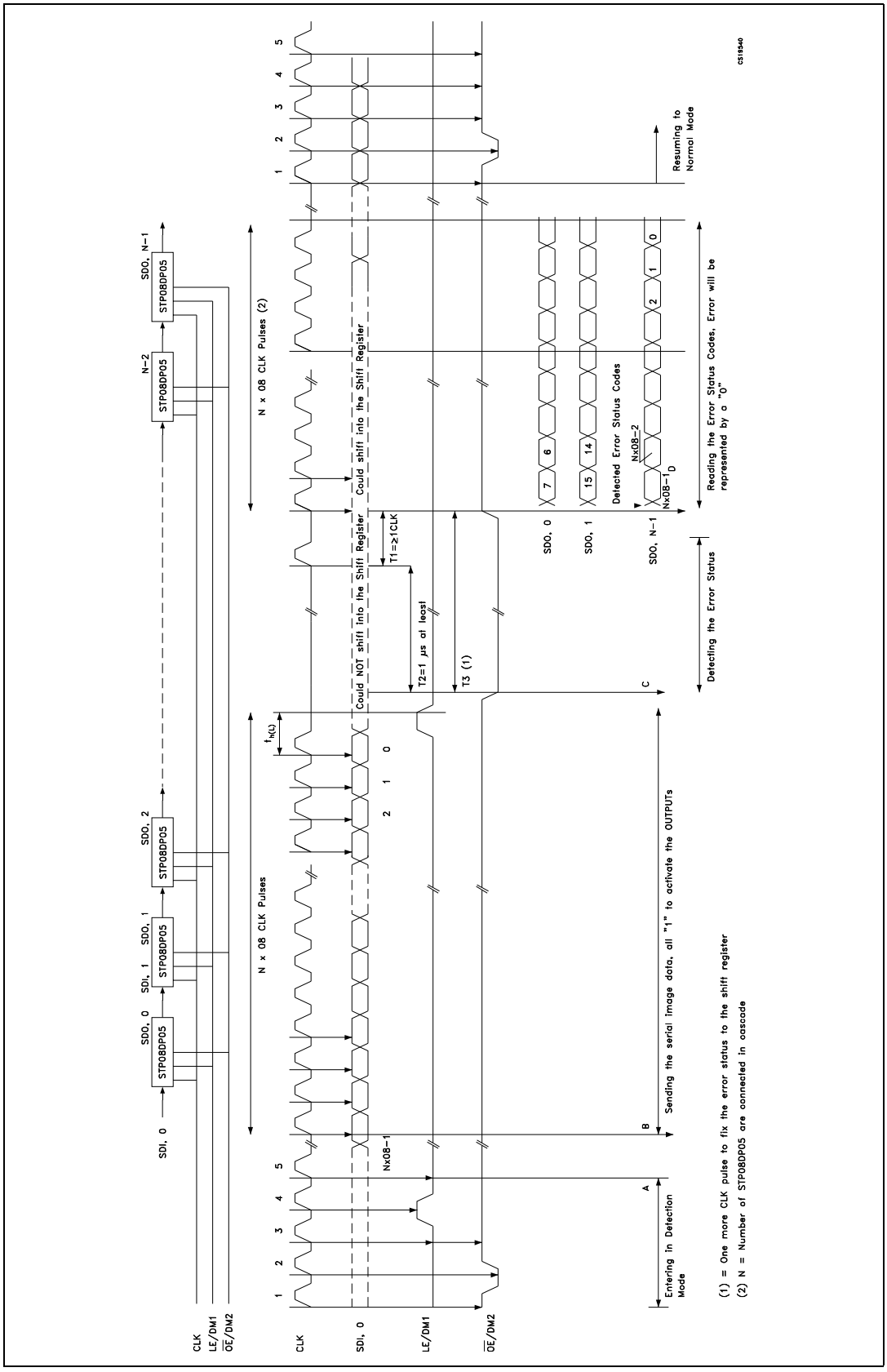


Figure 16. Timing example for open line and/or short detection



10 Detection mode functionality

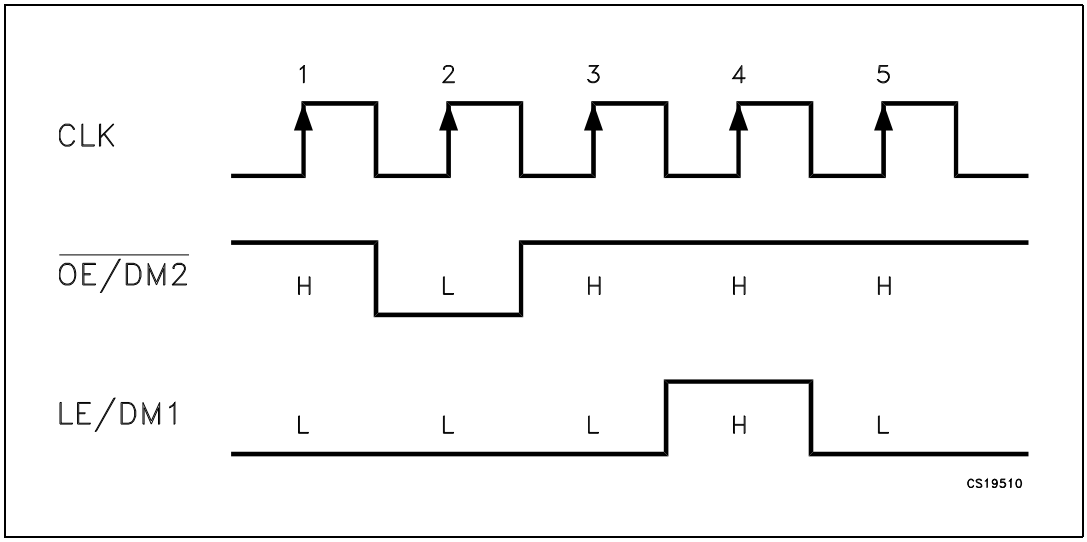
10.1 Phase one: “entering error detection mode“

From the “normal mode” condition the device can switch to “error detection mode” by a logic sequence on the $\overline{OE}$/DM2 and LE/DM1 pins as shown in the following table and diagram.

Table 12. Entering error detection mode truth table

CLK	1°	2°	3°	4°	5°
$\overline{OE}$/DM2	H	L	H	H	H
LE/DM1	L	L	L	H	L

Figure 17. Entering error detection mode timing diagram

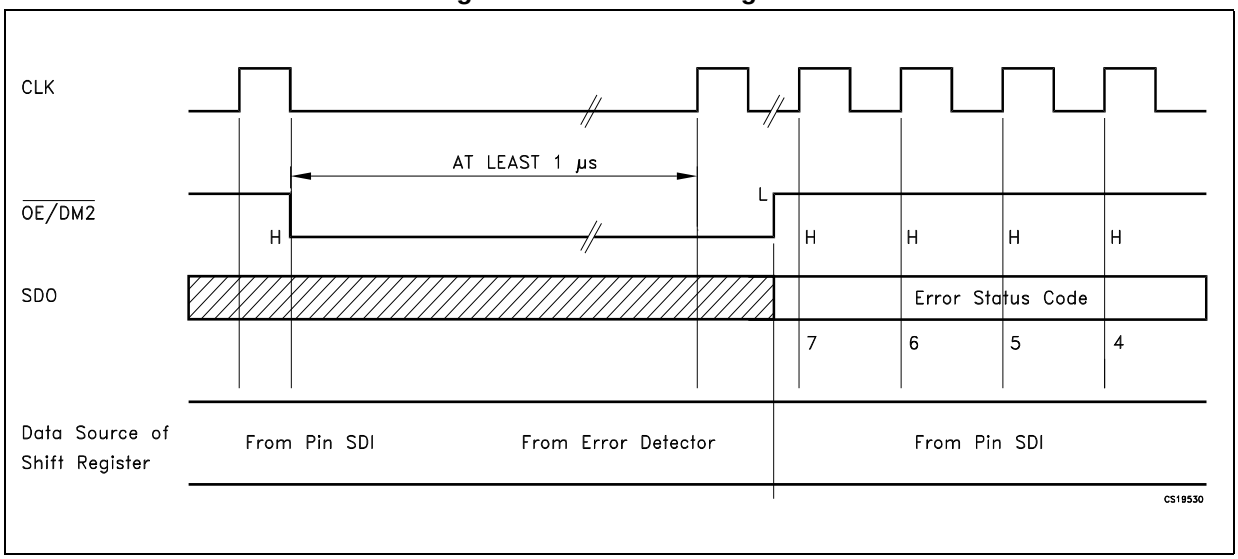


After these five CLK cycles the device goes into the “error detection mode” and at the 6th rising edge of CLK, the SDI data are ready for sampling.

10.2 Phase two: “error detection mode“

The eight data bits must be set to “1” in order to set ON all the outputs during detection. The data are latched by LE/DM1 and after that the outputs are ready for the detection process. When the microcontroller switches $\overline{OE}$/DM2 to LOW, the device drives the LEDs in order to analyze if an OPEN or SHORT condition has occurred.

Figure 18. Detection diagram



The status of the LEDs will be detected in 1 microsecond (minimum) and after this time the microcontroller sets *OE\DM2* in HIGH state and the output data detection result will go to the microprocessor via SDO.

Detection mode and normal mode both use the same data format. As soon as all the detection data bits are available on the serial line, the device may go back to normal mode of operation. To re-detect the status, the device must go back in normal mode and re-enter error detection mode.

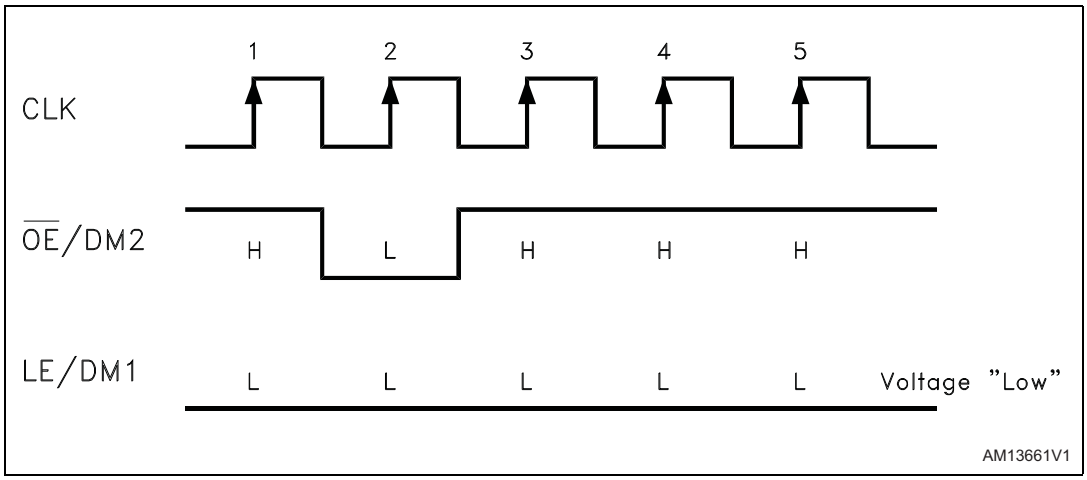
10.3 Phase three: “resuming normal mode”

The sequence for re-entering normal mode is shown in the following table and diagram.

Table 13. Resuming normal mode truth table

CLK	1°	2°	3°	4°	5°
$\overline{\text{OE}}$/DM2	H	L	H	H	H
LE/DM1	L	L	L	L	L

Figure 19. Resuming normal mode timing diagram



Note: For proper device operation the “entering error detection mode” sequence must be followed by a “resume mode” sequence, it is not possible to insert consecutive equal sequences.

10.4 Error detection conditions

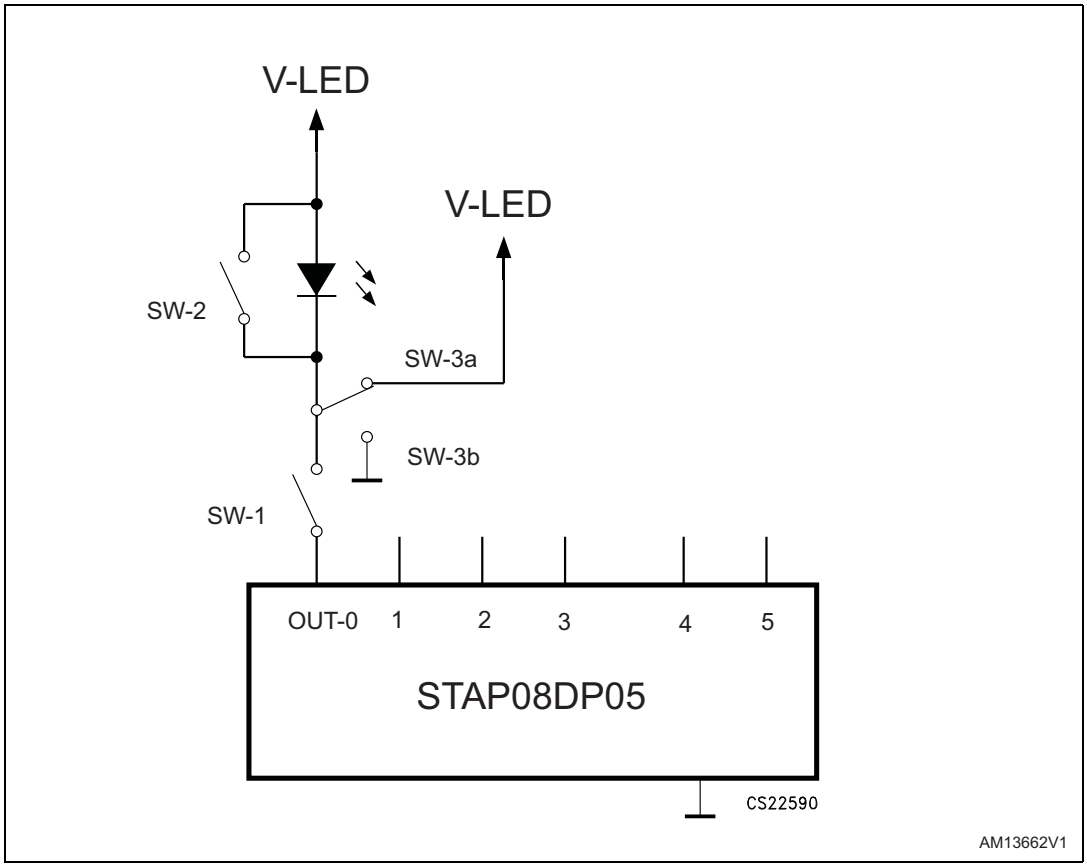
V_{DD} = 3.3 to 5 V temperature range 25 °C.

Table 14. Detection conditions

Configuration	Detect mode	Detection results		
SW-1 or SW-3b	Open line or output short to GND detected	==> $I_{ODEC} \leq 0.5 \times I_O$	No error detected	==> $I_{ODEC} \geq 0.5 \times I_O$
SW-2 or SW-3a	Short on LED or short to V-LED detected	==> $V_O \geq 2.5V$	No error detected	==> $V_O \leq 2.2$ V

Note: *Where:* I_O = the output current programmed by the R_{EXT}, I_{ODEC} = the detected output current in detection mode.

Figure 20. Detection circuit



11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

11.1 HTSSOP16 exposed pad package information

Figure 21. HTSSOP16 exposed pad package outline

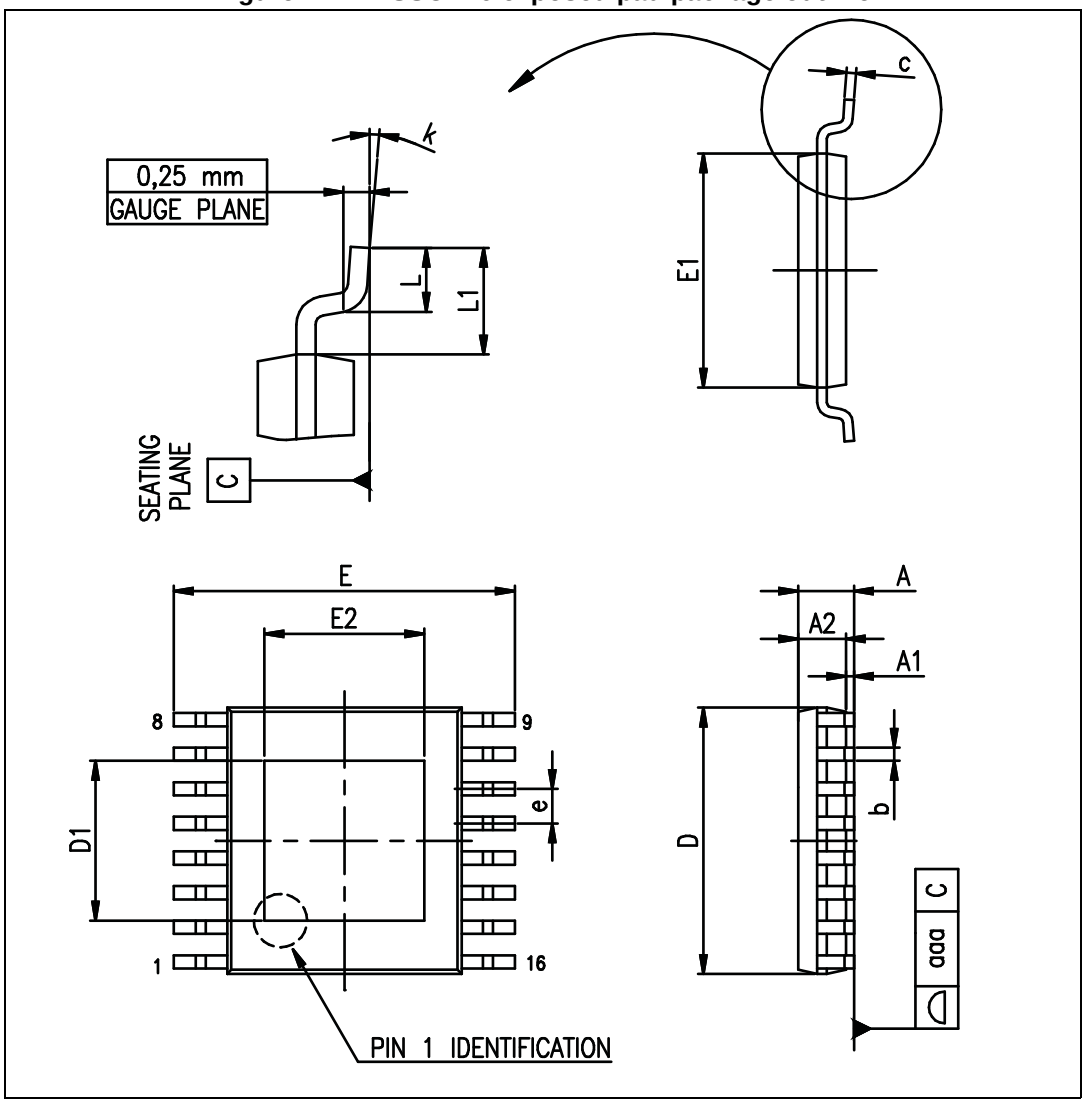


Table 15. HTSSOP16 exposed pad mechanical data

Dim.	(mm)		
	Min.	Typ.	Max.
A			1.20
A1			0.15
A2	0.80	1.00	1.05
b	0.19		0.30
c	0.09		0.20
D	4.90	5.00	5.10
D1	2.8	3	3.2
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2	2.8	3	3.2
e		0.65	
L	0.45	0.60	0.75
L1		1.00	
k	0.00		8.00
aaa			0.10

11.2 HTSSOP16 exposed pad packing information

Figure 22. HTSSOP16 tape and reel outline

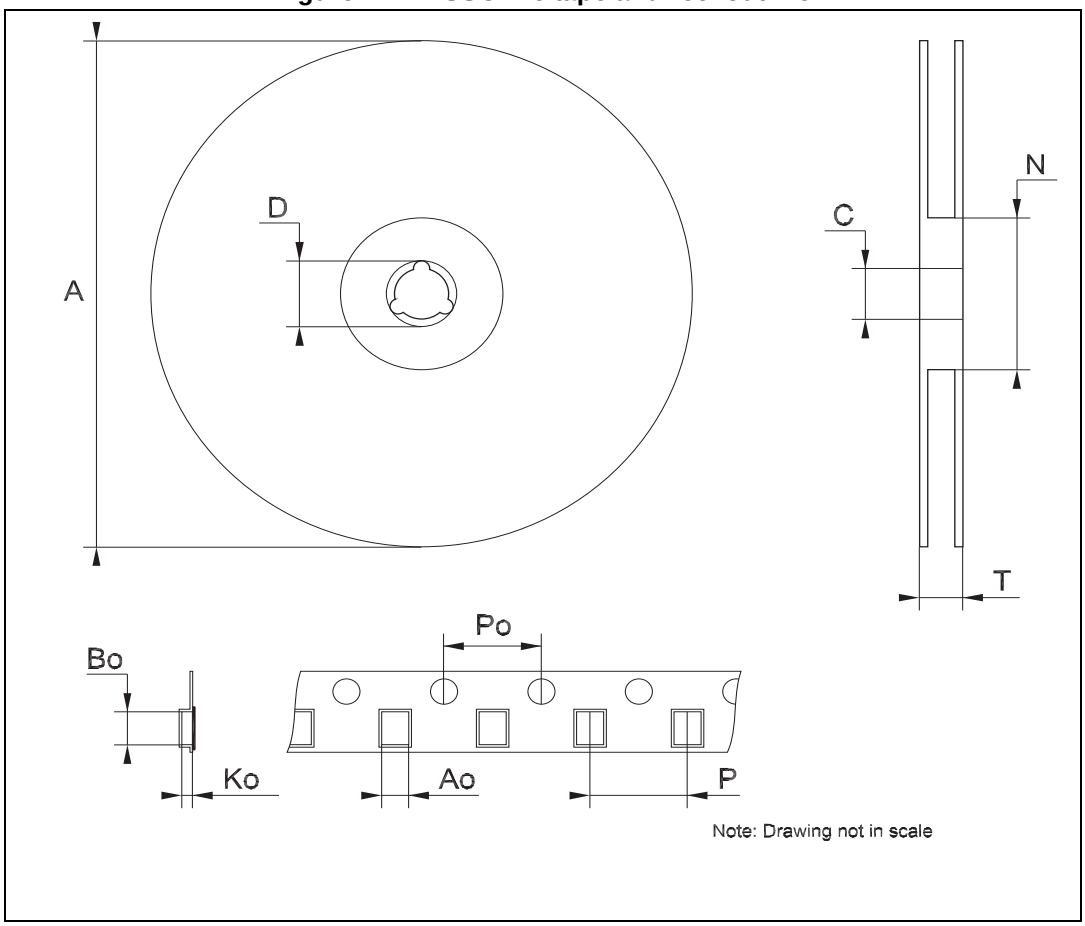


Table 16. HTSSOP16 tape and reel mechanical data

Dim.	(mm)		
	Min.	Typ.	Max.
A			330
C	12.8		13.2
D	20.2		
N	60		
T			22.4
Ao	6.7		6.9
Bo	5.3		5.5
Ko	1.6		1.8
Po	3.9		4.1
P	7.9		8.1

12 Revision history

Table 17. Document revision history

Date	Revision	Changes
12-Mar-2013	1	First release.
01-Jul-2013	2	Added footnote in Table 8: Switching characteristics.
11-Oct-2013	3	Modified TOPR value in Table 4: Absolute maximum ratings.
07-Jan-2014	4	Updated the Description in cover page, tablefootnote in Table 5: Thermal data, note in Figure 13: Power dissipation vs. package temperature, Figure 3: OE/DM2 terminal, Figure 4: LE/DM1 terminal, Figure 5: CLK, SDI terminal and Figure 6: SDO terminal.
06-Mar-2014	5	Modified footnote 1 in Table 8: Switching characteristics. Added footnote 2 in Table 8: Switching characteristics.
06-Nov-2015	6	Updated features in cover page. Minor text changes.