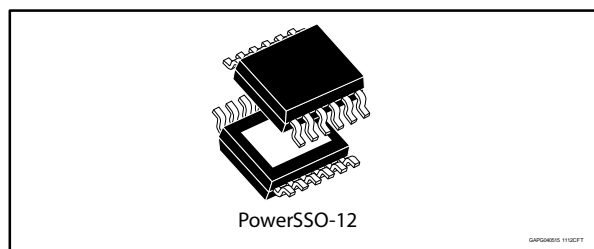


Double channel high-side driver with CurrentSense analog feedback for automotive applications

Datasheet - production data



Features

| | | |
|--|---------------------|----------------|
| Max transient supply voltage | V_{CC} | 40 V |
| Operating voltage range | V_{CC} | 4 V to 28 V |
| Minimum cranking supply voltage (V_{CC} decreasing) | $V_{USD_Cranking}$ | 2.85 V |
| Typ. on-state resistance (per Ch) | R_{ON} | 140 m Ω |
| Current limitation (typ) | I_{LIMH} | 12 A |
| Standby current (max) | I_{STBY} | 0.5 μ A |

- Automotive qualified
- Extreme low voltage operation for deep cold cranking applications (compliant with LV124, revision 2013)
- General
 - Double channel smart high-side driver with CurrentSense analog feedback
 - Very low standby current
 - Compatible with 3 V and 5 V CMOS outputs
- CurrentSense diagnostic functions
 - Multiplexed analog feedback of: load current with high precision proportional current mirror
 - Overload and short to ground (power limitation) indication
 - Thermal shutdown indication
 - Off-state open-load detection
 - Output short to V_{CC} detection

- Sense enable/ disable
- Protections
 - Undervoltage shutdown
 - Overvoltage clamp
 - Load current limitation
 - Self limiting of fast thermal transients
 - Loss of ground and loss of V_{CC}
 - Reverse battery with external components
 - Electrostatic discharge protection

Applications

- All types of automotive resistive, inductive and capacitive loads
- Specially intended for automotive signal lamps (up to R10W or LED Rear Combinations)

Description

The device is a double channel high-side driver manufactured using ST proprietary VIPower[®] technology and housed in PowerSSO-12 package. The device is designed to drive 12 V automotive grounded loads through a 3 V and 5 V CMOS compatible interface, providing protection and diagnostics.

The device integrates advanced protective functions such as load current limitation, overload active management by power limitation and overtemperature shutdown.

A current sense delivers high precision proportional load current sense in addition to the detection of overload and short circuit to ground, short to V_{CC} and off-state open-load.

A sense enable pin allows off-state diagnosis to be disabled during the module low-power mode as well as external sense resistor sharing among similar devices.

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1 Block diagram and pin description

Figure 1: Block diagram

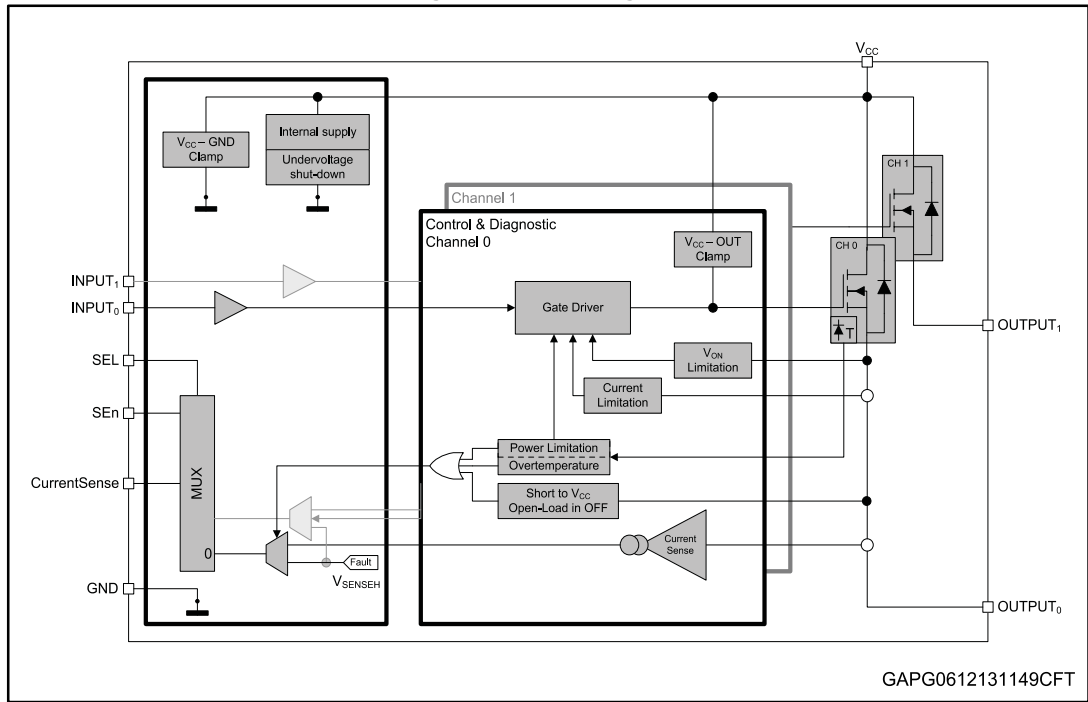


Table 1: Pin functions

| Name | Function |
|-----------------------|--|
| V _{CC} | Battery connection. |
| OUTPUT _{0,1} | Power output. |
| GND | Ground connection. Must be reverse battery protected by an external diode/resistor network. |
| INPUT _{0,1} | Voltage controlled input pins with hysteresis, compatible with 3 V and 5 V CMOS outputs. They control output switch state. |
| CurrentSense | Multiplexed analog sense output pin; it delivers a current proportional to the load current. |
| SEn | Active high compatible with 3 V and 5 V CMOS outputs pin; it enables the CurrentSense diagnostic pin. |
| SEL | Active high compatible with 3 V and 5 V CMOS outputs pin; it addresses the CurrentSense multiplexer. |

Figure 2: Configuration diagram (top view)

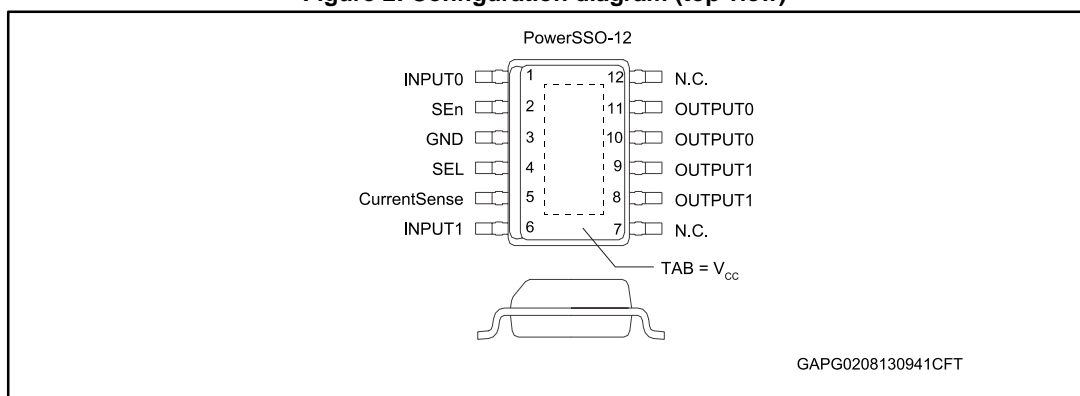


Table 2: Suggested connections for unused and not connected pins

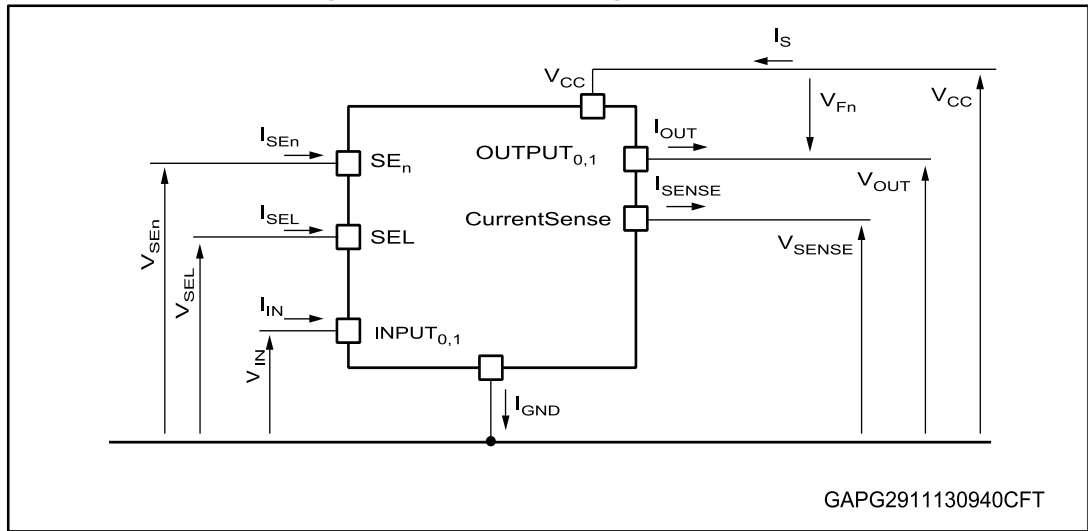
| Connection/pin | CurrentSense | N.C. | Output | Input | SE_n, SEL |
|----------------|-----------------------|------------------|-------------|------------------------|------------------------|
| Floating | Not allowed | X ⁽¹⁾ | X | X | X |
| To ground | Through 1 kΩ resistor | X | Not allowed | Through 15 kΩ resistor | Through 15 kΩ resistor |

Notes:

⁽¹⁾X: do not care.

2 Electrical specification

Figure 3: Current and voltage conventions



$V_{Fn} = V_{OUTn} - V_{CC}$ during reverse battery condition.

2.1 Absolute maximum ratings

Stressing the device above the rating listed in [Table 3: "Absolute maximum ratings"](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

Table 3: Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|-------------|---|--------------------|------|
| V_{CC} | DC supply voltage | 38 | V |
| $-V_{CC}$ | Reverse DC supply voltage | 0.3 | V |
| V_{CCPK} | Maximum transient supply voltage (ISO 16750-2:2010 Test B clamped to 40 V; $R_L = 4 \Omega$) | 40 | V |
| V_{CCJS} | Maximum jump start voltage for single pulse short circuit protection | 28 | V |
| $-I_{GND}$ | DC reverse ground pin current | 200 | mA |
| I_{OUT} | OUTPUT _{0,1} DC output current | Internally limited | A |
| $-I_{OUT}$ | Reverse DC output current | 4 | |
| I_{IN} | INPUT _{0,1} DC input current | -1 to 10 | mA |
| I_{SEn} | SEn DC input current | | |
| I_{SEL} | SEL DC input current | | |
| I_{SENSE} | CurrentSense pin DC output current ($V_{GND} = V_{CC}$ and $V_{SENSE} < 0 V$) | 10 | mA |
| | CurrentSense pin DC output current in reverse ($V_{CC} < 0V$) | -20 | |

| Symbol | Parameter | Value | Unit |
|-----------|---|------------|------|
| E_{MAX} | Maximum switching energy (single pulse) ($T_{DEMAG} = 0.4 \text{ ms}$; $T_{jstart} = 150 \text{ }^\circ\text{C}$) | 10 | mJ |
| V_{ESD} | Electrostatic discharge (JEDEC 22A-114F) | | |
| | • INPUT _{0,1} | 4000 | V |
| | • CurrentSense | 2000 | V |
| | • SEn, SEL | 4000 | V |
| | • OUTPUT _{0,1} | 4000 | V |
| | • V _{CC} | 4000 | V |
| V_{ESD} | Charge device model (CDM-AEC-Q100-011) | 750 | V |
| T_j | Junction operating temperature | -40 to 150 | °C |
| T_{stg} | Storage temperature | -55 to 150 | |

2.2 Thermal data

Table 4: Thermal data

| Symbol | Parameter | Typ. value | Unit |
|-----------------|--|------------|------|
| $R_{thj-board}$ | Thermal resistance junction-board (JEDEC JESD 51-5 / 51-8) ⁽¹⁾⁽²⁾ | 7.7 | °C/W |
| $R_{thj-amb}$ | Thermal resistance junction-ambient (JEDEC JESD 51-5) ⁽¹⁾⁽³⁾ | 61 | |
| $R_{thj-amb}$ | Thermal resistance junction-ambient (JEDEC JESD 51-7) ⁽¹⁾⁽²⁾ | 26.5 | |

Notes:

⁽¹⁾One channel ON.

⁽²⁾Device mounted on four-layers 2s2p PCB.

⁽³⁾Device mounted on two-layers 2s0p PCB with 2 cm² heatsink copper trace.

2.3 Main electrical characteristics

7 V < V_{CC} < 28 V; -40 °C < T_j < 150 °C, unless otherwise specified.

All typical values refer to V_{CC} = 13 V; T_j = 25°C, unless otherwise specified.

Table 5: Electrical characteristics during cranking

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------------------|--|---|------|------|------|------|
| $V_{USD_Cranking}$ | Minimum cranking supply voltage (V _{CC} decreasing) | | | | 2.85 | V |
| R_{ON} | On-state resistance ⁽¹⁾ | I _{OUT} = 0.2 A; V _{CC} = 2.85 V; V _{CC} decreasing | | | 1400 | mΩ |
| T_{TSD} ⁽²⁾ | Shutdown temperature (V _{CC} decreasing) | V _{CC} = 2.85 V | 140 | | | °C |

Notes:

⁽¹⁾For each channel.

⁽²⁾Parameter guaranteed by design and characterization; not subject to production test.

Table 6: Power section

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------------|---|--|------|------|------|------|
| V _{CC} | Operating supply voltage | | 4 | 13 | 28 | V |
| V _{USD} | Undervoltage shutdown | | | | 2.85 | |
| V _{USDReset} | Undervoltage shutdown reset | | | | 5 | |
| V _{USDhyst} | Undervoltage shutdown hysteresis | | | 0.3 | | |
| R _{ON} | On-state resistance ⁽¹⁾ | I _{OUT} = 1 A; T _j = 25 °C | | 140 | | mΩ |
| | | I _{OUT} = 1 A; T _j = 150 °C | | | 280 | |
| | | I _{OUT} = 1 A; V _{CC} = 4 V; T _j = 25 °C | | | 210 | |
| V _{clamp} | Clamp voltage | I _S = 20 mA; T _j = -40 °C | 38 | | | V |
| | | I _S = 20 mA; 25°C < T _j < 150°C | 41 | 46 | 52 | |
| I _{STBY} | Supply current in standby at V _{CC} = 13 V ⁽²⁾ | V _{CC} = 13 V; V _{IN} = V _{OUT} = V _{SEn} = 0 V; V _{SEL} = 0 V; T _j = 25 °C | | | 0.5 | μA |
| | | V _{CC} = 13 V; V _{IN} = V _{OUT} = V _{SEn} = 0 V; V _{SEL} = 0 V; T _j = 85 °C ⁽³⁾ | | | 0.5 | μA |
| | | V _{CC} = 13 V; V _{IN} = V _{OUT} = V _{SEn} = 0 V; V _{SEL} = 0 V; T _j = 125 °C | | | 3 | μA |
| t _{D_STBY} | Standby mode blanking time | V _{CC} = 13 V; V _{IN} = V _{OUT} = V _{SEL} = 0 V; V _{SEn} = 5 V to 0 V | 60 | 300 | 550 | μA |
| I _{S(ON)} | Supply current | V _{CC} = 13 V; V _{SEn} = V _{SEL} = 0 V; V _{IN0} = 5 V; V _{IN1} = 5 V; I _{OUT0} = 0 A; I _{OUT1} = 0 A | | 5 | 8 | mA |
| I _{GND(ON)} | Control stage current consumption in ON state. All channels active. | V _{CC} = 13 V; V _{SEn} = 5 V; V _{SEL} = 0 V; V _{IN0} = 5 V; V _{IN1} = 5 V; I _{OUT0} = 1 A; I _{OUT1} = 1 A | | | 12 | mA |
| I _{L(off)} | Off-state output current at V _{CC} = 13 V ⁽¹⁾ | V _{IN} = V _{OUT} = 0 V; V _{CC} = 13 V; T _j = 25 °C | 0 | 0.01 | 0.5 | μA |
| | | V _{IN} = V _{OUT} = 0 V; V _{CC} = 13 V; T _j = 125 °C | 0 | | 3 | |
| V _F | Output - V _{CC} diode voltage ⁽¹⁾ | I _{OUT} = -1 A; T _j = 150 °C | | | 0.7 | V |

Notes:⁽¹⁾For each channel.⁽²⁾PowerMOS leakage included.⁽³⁾Parameter specified by design; not subject to production test.

Table 7: Switching

| V _{CC} = 13 V; -40°C < T _j < 150°C, unless otherwise specified | | | | | | |
|--|---|-----------------------|------|------|------|------|
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
| t _{d(on)} ⁽¹⁾ | Turn-on delay time at T _j = 25°C | R _L = 13 Ω | 10 | 70 | 120 | μs |
| t _{d(off)} ⁽¹⁾ | Turn-off delay time at T _j = 25°C | | 10 | 40 | 100 | |
| (dV _{OUT} /dt) _{on} ⁽¹⁾ | Turn-on voltage slope at T _j = 25°C | R _L = 13 Ω | 0.1 | 0.27 | 0.7 | V/μs |
| (dV _{OUT} /dt) _{off} ⁽¹⁾ | Turn-off voltage slope at T _j = 25°C | | 0.1 | 0.35 | 0.7 | |

| V _{CC} = 13 V; -40°C < T _j < 150°C, unless otherwise specified | | | | | | |
|--|--|-----------------------|------|------|---------------------|------|
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
| W _{ON} | Switching energy losses at turn-on (t _{won}) | R _L = 13 Ω | — | 0.15 | 0.18 ⁽²⁾ | mJ |
| W _{OFF} | Switching energy losses at turn-off (t _{woff}) | R _L = 13 Ω | — | 0.1 | 0.18 ⁽²⁾ | mJ |
| t _{SKEW} ⁽¹⁾ | Differential pulse skew (t _{PHL} - t _{PLH}) | R _L = 13 Ω | -100 | -50 | 0 | µs |

Notes:

⁽¹⁾See [Figure 6: "Switching times and Pulse skew"](#)

⁽²⁾Parameter guaranteed by design and characterization; not subject to production test.

Table 8: Logic inputs

| 7 V < V _{CC} < 28 V; -40°C < T _j < 150°C | | | | | | |
|--|--------------------------|-------------------------|------|------|------|------|
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
| INPUT_{0,1} characteristics | | | | | | |
| V _{IL} | Input low level voltage | | | | 0.9 | V |
| I _{IL} | Low level input current | V _{IN} = 0.9 V | 1 | | | µA |
| V _{IH} | Input high level voltage | | 2.1 | | | V |
| I _{IH} | High level input current | V _{IN} = 2.1 V | | | 10 | µA |
| V _{I(hyst)} | Input hysteresis voltage | | 0.2 | | | V |
| V _{ICL} | Input clamp voltage | I _{IN} = 1 mA | 5.3 | | 7.2 | V |
| | | I _{IN} = -1 mA | | -0.7 | | |
| SEL characteristics (7 V < V_{CC} < 18 V) | | | | | | |
| V _{SELL} | Input low level voltage | | | | 0.9 | V |
| I _{SELL} | Low level input current | V _{IN} = 0.9 V | 1 | | | µA |
| V _{SELH} | Input high level voltage | | 2.1 | | | V |
| I _{SELH} | High level input current | V _{IN} = 2.1 V | | | 10 | µA |
| V _{SEL(hyst)} | Input hysteresis voltage | | 0.2 | | | V |
| V _{SELCL} | Input clamp voltage | I _{IN} = 1 mA | 5.3 | | 7.2 | V |
| | | I _{IN} = -1 mA | | -0.7 | | |
| SEn characteristics (7 V < V_{CC} < 18 V) | | | | | | |
| V _{SEnL} | Input low level voltage | | | | 0.9 | V |
| I _{SEnL} | Low level input current | V _{IN} = 0.9 V | 1 | | | µA |
| V _{SEnH} | Input high level voltage | | 2.1 | | | V |
| I _{SEnH} | High level input current | V _{IN} = 2.1 V | | | 10 | µA |
| V _{SEn(hyst)} | Input hysteresis voltage | | 0.2 | | | V |
| V _{SEnCL} | Input clamp voltage | I _{IN} = 1 mA | 5.3 | | 7.2 | V |
| | | I _{IN} = -1 mA | | -0.7 | | |

Table 9: Protections

| 7 V < V _{CC} < 18 V; -40°C < T _j < 150°C | | | | | | |
|--|--|---|----------------------|----------------------|----------------------|------|
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
| I _{LIMH} | DC short circuit current | V _{CC} = 13 V | 8 | 12 | 16 | A |
| | | 4 V < V _{CC} < 18 V ⁽¹⁾ | | | 16 | |
| I _{LIML} | Short circuit current during thermal cycling | V _{CC} = 13 V; T _R < T _j < T _{TSD} | | 4 | | |
| T _{TSD} | Shutdown temperature | | 150 | 175 | 200 | °C |
| T _R | Reset temperature ⁽¹⁾ | | T _{RS} + 1 | T _{RS} + 7 | | |
| T _{RS} | Thermal reset of fault diagnostic indication | V _{SEn} = 5 V | 135 | | | |
| T _{HYST} | Thermal hysteresis (T _{TSD} - T _R) ⁽¹⁾ | | | 7 | | |
| ΔT _{J,SD} | Dynamic temperature | T _j = -40 °C; V _{CC} = 13 V | | 60 | | K |
| V _{DEMAG} | Turn-off output voltage clamp | I _{OUT} = 1 A; L = 6 mH; T _j = -40 °C | V _{CC} - 38 | | | V |
| | | I _{OUT} = 1 A; L = 6 mH; T _j = 25 °C to +150 °C | V _{CC} - 41 | V _{CC} - 46 | V _{CC} - 52 | |
| V _{ON} | Output voltage drop limitation | I _{OUT} = 0.07 A | | 20 | | mV |

Notes:

⁽¹⁾Parameter guaranteed by design and characterization; not subject to production test.

Table 10: CurrentSense

| 7 V < V _{CC} < 18 V; -40°C < T _j < 150°C | | | | | | |
|--|--|--|------|------|------|------|
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
| V _{SENSE_CL} | CurrentSense clamp voltage | V _{SEn} = 0 V; I _{SENSE} = 1 mA | -17 | | -12 | V |
| | | V _{SEn} = 0 V; I _{SENSE} = -1 mA | | 7 | | V |
| CurrentSense characteristics | | | | | | |
| K _{OL} | I _{OUT} /I _{SENSE} | I _{OUT} = 0.01 A; V _{SENSE} = 0.5 V; V _{SEn} = 5 V | 295 | | | |
| dK _{cal} /K _{cal} ⁽¹⁾⁽²⁾ | Current sense ratio drift at calibration point | I _{OUT} = 0.01 A to 0.025 A; I _{cal} = 17.5 mA; V _{SENSE} = 0.5 V; V _{SEn} = 5 V | -30 | | 30 | % |
| K _{LED} | I _{OUT} /I _{SENSE} | I _{OUT} = 0.025 A; V _{SENSE} = 0.5 V; V _{SEn} = 5 V | 330 | 580 | 820 | |
| dK _{LED} /K _{LED} ⁽¹⁾⁽²⁾ | Current sense ratio drift | I _{OUT} = 0.025 A; V _{SENSE} = 0.5 V; V _{SEn} = 5 V | -25 | | 25 | % |
| K ₀ | I _{OUT} /I _{SENSE} | I _{OUT} = 0.07 A; V _{SENSE} = 0.5 V; V _{SEn} = 5 V | 375 | 550 | 720 | |
| dK ₀ /K ₀ ⁽¹⁾⁽²⁾ | Current sense ratio drift | I _{OUT} = 0.07 A; V _{SENSE} = 0.5 V; V _{SEn} = 5 V | -20 | | 20 | % |
| K ₁ | I _{OUT} /I _{SENSE} | I _{OUT} = 0.15 A; V _{SENSE} = 4 V; V _{SEn} = 5 V | 360 | 500 | 670 | |

| 7 V < V _{CC} < 18 V; -40°C < T _J < 150°C | | | | | | |
|--|--|---|------|------|------|------|
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
| dK ₁ /K ₁ ⁽¹⁾⁽²⁾ | Current sense ratio drift | I _{OUT} = 0.15 A; V _{SENSE} = 4 V; V _{SEN} = 5 V | -15 | | 15 | % |
| K ₂ | I _{OUT} /I _{SENSE} | I _{OUT} = 0.7 A; V _{SENSE} = 4 V; V _{SEN} = 5 V | 380 | 475 | 570 | |
| dK ₂ /K ₂ ⁽¹⁾⁽²⁾ | Current sense ratio drift | I _{OUT} = 0.7 A; V _{SENSE} = 4 V; V _{SEN} = 5 V | -10 | | 10 | % |
| K ₃ | I _{OUT} /I _{SENSE} | I _{OUT} = 2 A; V _{SENSE} = 4 V; V _{SEN} = 5 V | 430 | 470 | 520 | |
| dK ₃ /K ₃ ⁽¹⁾⁽²⁾ | Current sense ratio drift | I _{OUT} = 2 A; V _{SENSE} = 4 V; V _{SEN} = 5 V | -5 | | 5 | % |
| I _{SENSE0} | CurrentSense leakage current | CurrentSense disabled: V _{SEN} = 0 V | 0 | | 0.5 | μA |
| | | CurrentSense disabled: -1 V < V _{SENSE} < 5 V ⁽¹⁾ | -0.5 | | 0.5 | μA |
| | | CurrentSense enabled: V _{SEN} = 5 V; All channel ON; I _{OUTX} = 0 A; Ch _X diagnostic selected; • E.g. Ch ₀ : V _{IN0} = 5 V; V _{IN1} = 5 V; V _{SEL} = 0 V; I _{OUT0} = 0 A; I _{OUT1} = 1 A | 0 | | 2 | μA |
| | | CurrentSense enabled: V _{SEN} = 5 V; Ch _X channel OFF; Ch _X diagnostic selected; • E.g. Ch ₀ : V _{IN0} = 0 V; V _{IN1} = 5 V; V _{SEL} = 0 V; I _{OUT1} = 1 A | 0 | | 2 | μA |
| V _{OUT_MSD} ⁽¹⁾ | Output Voltage for CurrentSense shutdown | V _{SEN} = 5 V; R _{SENSE} = 2.7 kΩ • E.g. Ch ₀ : V _{IN0} = 5 V; V _{SEL} = 0 V; I _{OUT0} = 1 A | | 5 | | V |
| V _{SENSE_SAT} | CurrentSense saturation voltage | V _{CC} = 7 V; R _{SENSE} = 2.7 kΩ; V _{SEN} = 5 V; V _{IN0} = 5 V; V _{SEL} = 0 V; I _{OUT0} = 1 A; T _J = 150°C | 5 | | | V |
| I _{SENSE_SAT} ⁽¹⁾ | CS saturation current | V _{CC} = 7 V; V _{SENSE} = 4 V; V _{IN0} = 5 V; V _{SEN} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = 0 V; T _J = 150°C | 4 | | | mA |

| 7 V < V _{CC} < 18 V; -40°C < T _j < 150°C | | | | | | |
|---|---|--|------|------|------|------|
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
| I _{OUT_SAT} ⁽¹⁾ | Output saturation current | V _{CC} = 7 V; V _{SENSE} = 4 V; V _{IN0} = 5 V; V _{SEn} = 5 V; V _{SEL} = 0 V; T _j = 150°C | 2.2 | | | A |
| Off-state diagnostic | | | | | | |
| V _{OL} | Off-state open-load voltage detection threshold | V _{SEn} = 5 V; Ch _X OFF; Ch _X diagnostic selected • E.g: Ch ₀ V _{IN0} = 0 V; V _{SEL} = 0 V | 2 | 3 | 4 | V |
| I _{L(off2)} | Off-state output sink current | V _{IN} = 0 V; V _{OUT} = V _{OL} ; T _j = -40 °C to 125 °C | -100 | | -15 | μA |
| t _{DSTKON} | Off-state diagnostic delay time from falling edge of INPUT (see Figure 8: "TDSTKON") | V _{SEn} = 5 V; Ch _X ON to OFF transition Ch _X diagnostic selected • E.g: Ch ₀ V _{IN0} = 5 V to 0 V; V _{SEL} = 0 V; I _{OUT0} = 0 A; V _{OUT} = 4 V | 100 | 350 | 700 | μs |
| t _{D_OL_V} | Settling time for valid OFF-state open load diagnostic indication from rising edge of SEn | V _{IN0} = 0 V; V _{IN1} = 0 V; V _{SEL} = 0 V; V _{OUT0} = 4 V; V _{SEn} = 0 V to 5 V | | | 60 | μs |
| t _{D_VOL} | Off-state diagnostic delay time from rising edge of V _{OUT} | V _{SEn} = 5 V; Ch _X OFF Ch _X diagnostic selected • E.g: Ch ₀ V _{IN0} = 0 V; V _{SEL} = 0 V; V _{OUT} = 0 V to 4 V | | 5 | 30 | μs |
| Fault diagnostic feedback (see Table 11: "Truth table") | | | | | | |
| V _{SENSEH} | CurrentSense output voltage in fault condition | V _{CC} = 13 V; R _{SENSE} = 1 kΩ • E.g: Ch ₀ in open load V _{IN0} = 0 V; V _{SEn} = 5 V; V _{SEL} = 0 V; I _{OUT0} = 0 A; V _{OUT} = 4 V | 5 | | 6.6 | V |
| I _{SENSEH} | CurrentSense output current in fault condition | V _{CC} = 13 V; V _{SENSE} = 5 V | 7 | 20 | 30 | mA |
| CurrentSense timings (current sense mode - see Figure 7: "CurrentSense timings")⁽³⁾ | | | | | | |
| t _{DSSENSE1H} | Current sense settling time from rising edge of SEn | V _{IN} = 5 V; V _{SEn} = 0 V to 5 V; R _{SENSE} = 1 kΩ; R _L = 13 Ω | | | 60 | μs |
| t _{DSSENSE1L} | Current sense disable delay time from falling edge of SEn | V _{IN} = 5 V; V _{SEn} = 5 V to 0 V; R _{SENSE} = 1 kΩ; R _L = 13 Ω | | 5 | 20 | μs |

| 7 V < V _{CC} < 18 V; -40°C < T _j < 150°C | | | | | | |
|--|---|--|------|------|------|------|
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
| t _{DSSENSE2H} | Current sense settling time from rising edge of INPUT | V _{IN} = 0 V to 5 V; V _{SEN} = 5 V; R _{SENSE} = 1 kΩ; R _L = 13 Ω | | 100 | 250 | μs |
| Δt _{DSSENSE2H} | Current sense settling time from rising edge of I _{OUT} (dynamic response to a step change of I _{OUT}) | V _{IN} = 5 V; V _{SEN} = 5 V; R _{SENSE} = 1 kΩ; I _{SENSE} = 90 % of I _{SENSEMAX} ; R _L = 13 Ω | | | 100 | μs |
| t _{DSSENSE2L} | Current sense turn-off delay time from falling edge of INPUT | V _{IN} = 5 V to 0 V; V _{SEN} = 5 V; R _{SENSE} = 1 kΩ; R _L = 13 Ω | | 50 | 250 | μs |
| CurrentSense timings (Multiplexer transition times) ⁽³⁾ | | | | | | |
| t _{D_XtoY} | CurrentSense transition delay from Ch _X to Ch _Y | V _{IN0} = 5 V; V _{IN1} = 5 V; V _{SEN} = 5 V; V _{SEL} = 0 V to 5 V; I _{OUT0} = 0 A; I _{OUT1} = 1 A; R _{SENSE} = 1 kΩ | | | 20 | μs |
| t _{D_CSstoVSENSEH} | CurrentSense transition delay from stable current sense on Ch _X to V _{SENSEH} on Ch _Y | V _{IN0} = 5 V; V _{IN1} = 0 V; V _{SEN} = 5 V; V _{SEL} = 0 V to 5 V; I _{OUT0} = 1 A; V _{OUT1} = 4 V; R _{SENSE} = 1 kΩ | | | 60 | μs |

Notes:

- (1)Parameter guaranteed by design and characterization; not subject to production test.
(2)All values refer to V_{CC} = 13 V; T_j = 25°C, unless otherwise specified.
(3)Transition delays are measured up to +/- 10% of final conditions.

Figure 4: IO_{UT}/ISENSE versus IO_{UT}

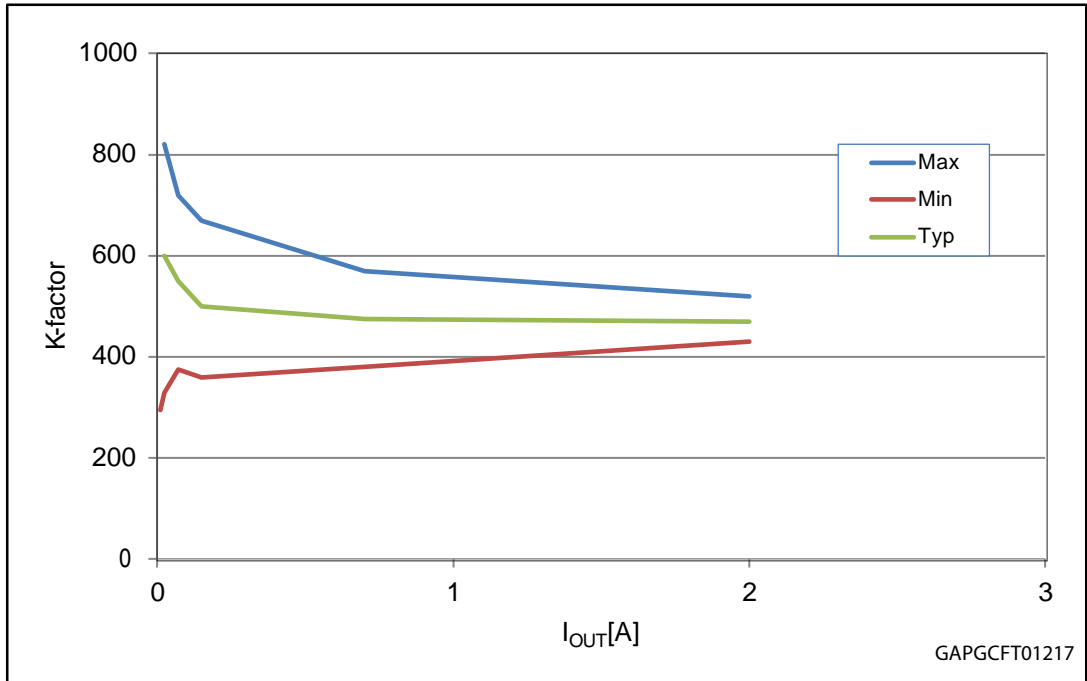


Figure 5: Current sense accuracy versus IO_{UT}

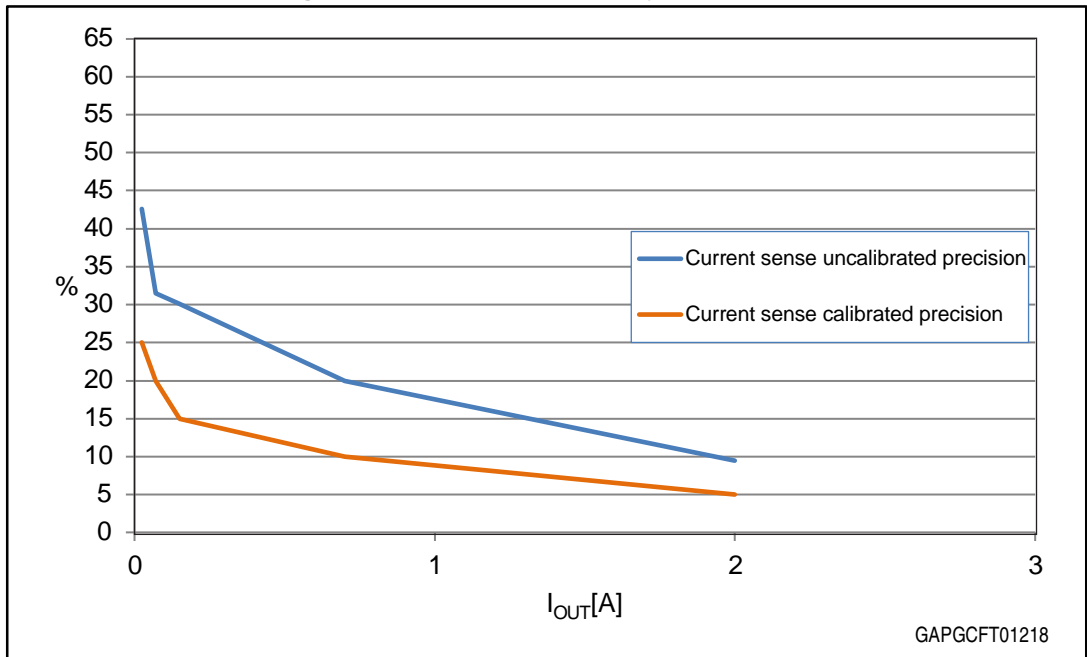


Figure 6: Switching times and Pulse skew

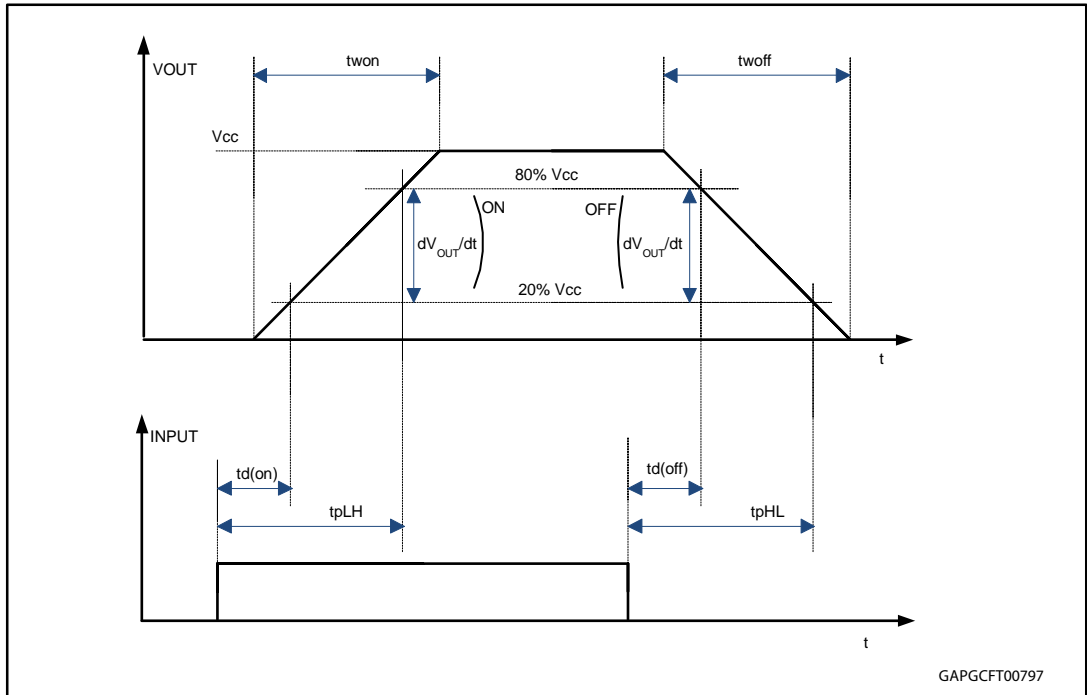


Figure 7: CurrentSense timings

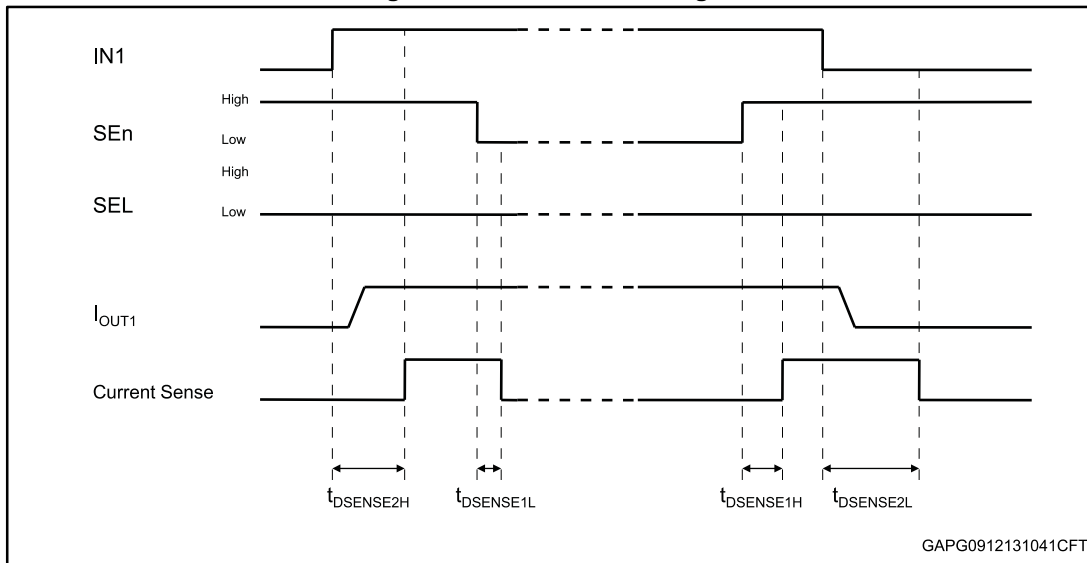


Figure 8: TDSTKON

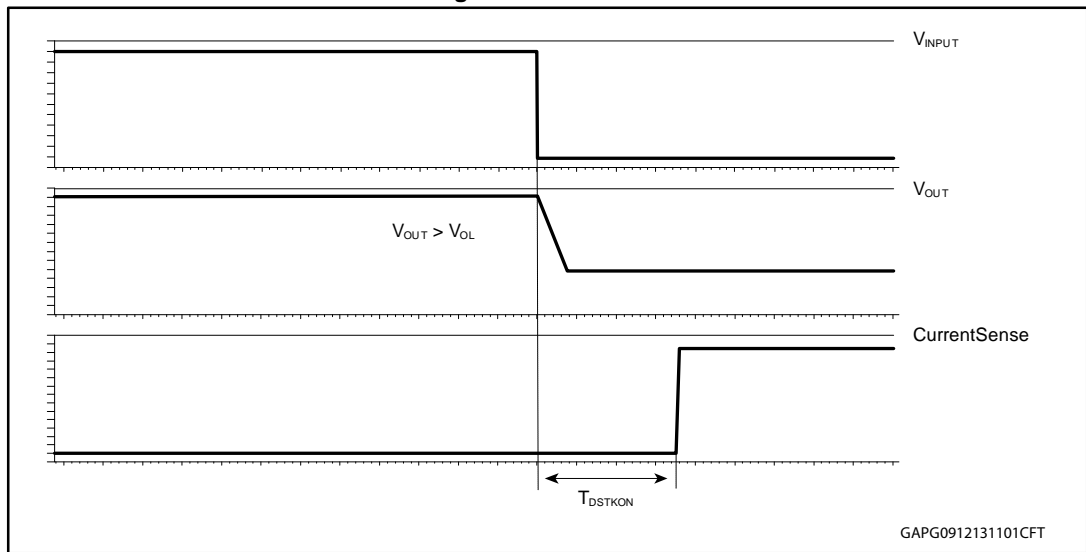


Table 11: Truth table

| Mode | Conditions | IN _x | SEn | SEL | OUT _x | CurrentSense | Comments |
|-------------------------|--|-----------------|---------|-----|------------------|--------------|---|
| Standby | All logic inputs low | L | L | L | L | Hi-Z | Low quiescent current consumption |
| Normal | Nominal load connected; $T_j < 150^\circ\text{C}$ | L | See (1) | | L | See (1) | |
| | | H | | | H | See (1) | Outputs configured for auto-restart |
| | | H | | | H | See (1) | Outputs configured for latch off |
| Overload | Overload or short to GND causing: $T_j > T_{TSD}$ or $\Delta T_j > \Delta T_{j_SD}$ | L | See (1) | | L | See (1) | |
| | | H | | | H | See (1) | Output cycles with temperature hysteresis |
| | | H | | | L | See (1) | Output latches off |
| Under-voltage | $V_{CC} < V_{USD}$ (falling) | X | X | X | L L | Hi-Z Hi-Z | Re-start when $V_{CC} > V_{USD} + V_{USDhyst}$ (rising) |
| Off-state diagnostics | Short to V_{CC} | L | See (1) | | H | See (1) | |
| | Open-load | L | | | H | See (1) | External pull up |
| Negative output voltage | Inductive loads turn-off | L | See (1) | | $< 0\text{ V}$ | See (1) | |

Notes:

(1) Refer to [Table 12: "CurrentSense multiplexer addressing"](#)

Table 12: CurrentSense multiplexer addressing

| SEn | SEL | MUX channel | CurrentSense output | | | |
|-----|-----|----------------------|------------------------------|--------------------------|--------------------------|-----------------|
| | | | Normal mode | Overload | Off-state diag. | Negative output |
| L | X | | Hi-Z | | | |
| H | L | Channel 0 diagnostic | $I_{SENSE} = 1/K * I_{OUT0}$ | $V_{SENSE} = V_{SENSEH}$ | $V_{SENSE} = V_{SENSEH}$ | Hi-Z |
| H | H | Channel 1 diagnostic | $I_{SENSE} = 1/K * I_{OUT1}$ | $V_{SENSE} = V_{SENSEH}$ | $V_{SENSE} = V_{SENSEH}$ | Hi-Z |

2.4 Waveforms

Figure 9: Standby mode activation

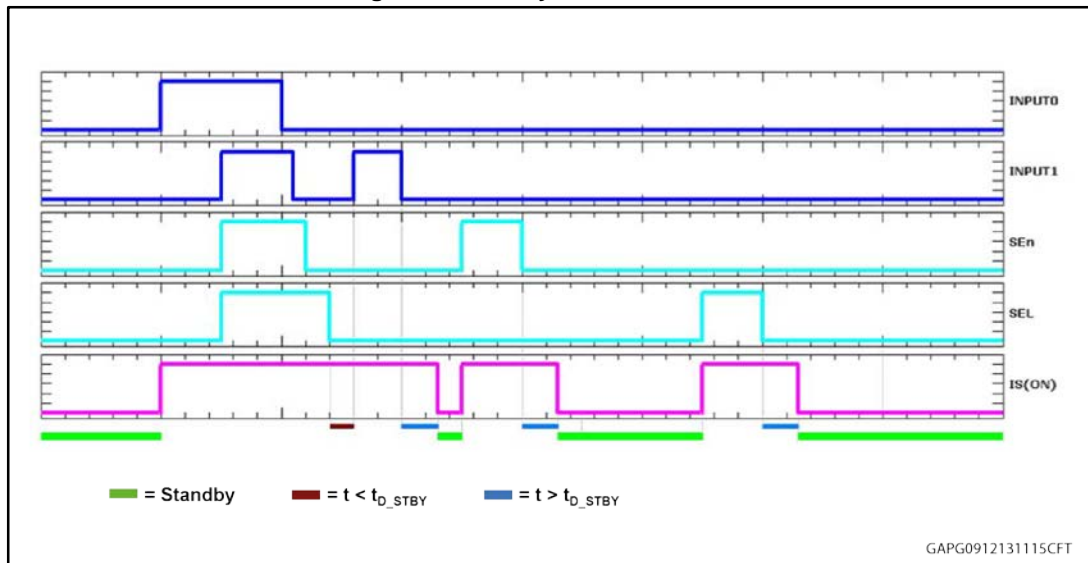
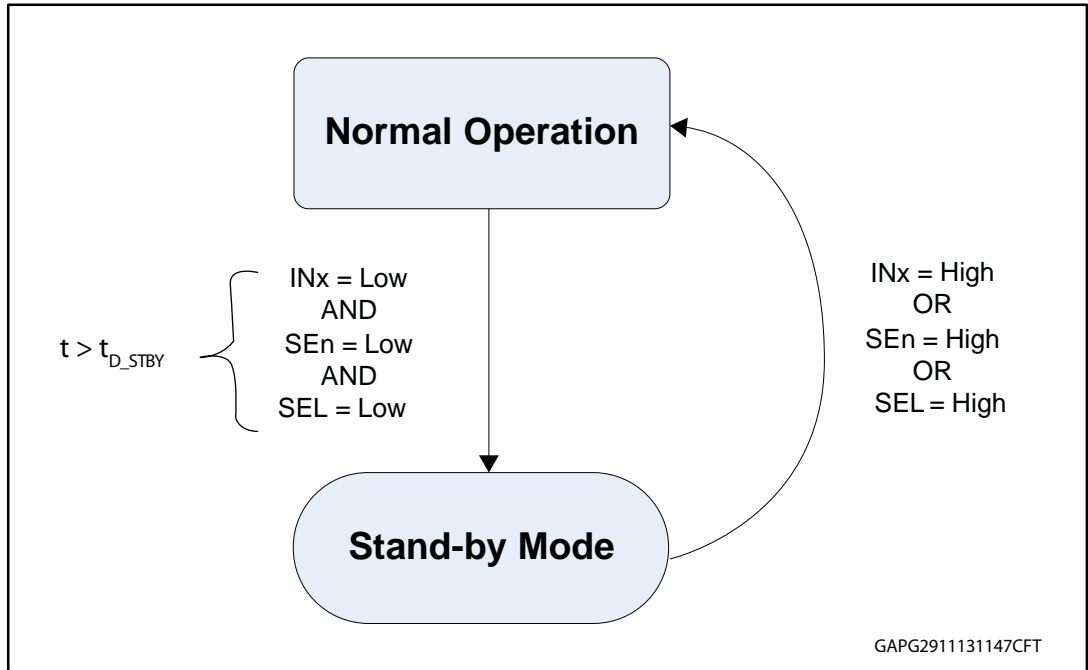
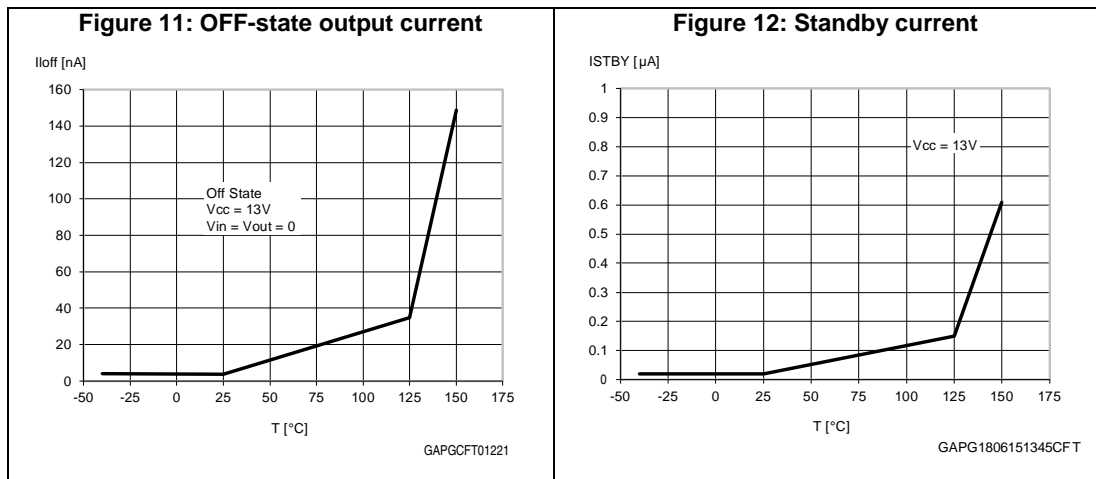


Figure 10: Standby state diagram



2.5 Electrical characteristics curves



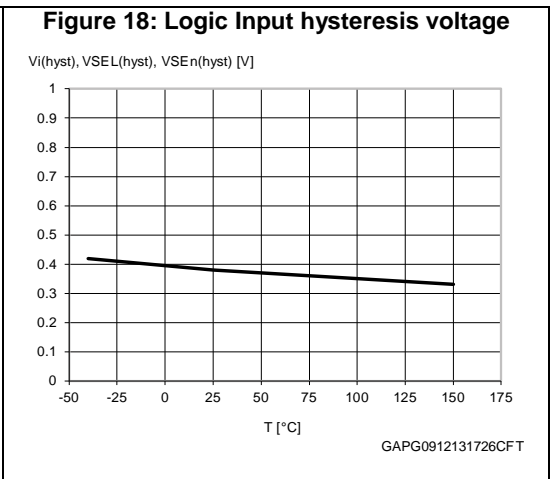
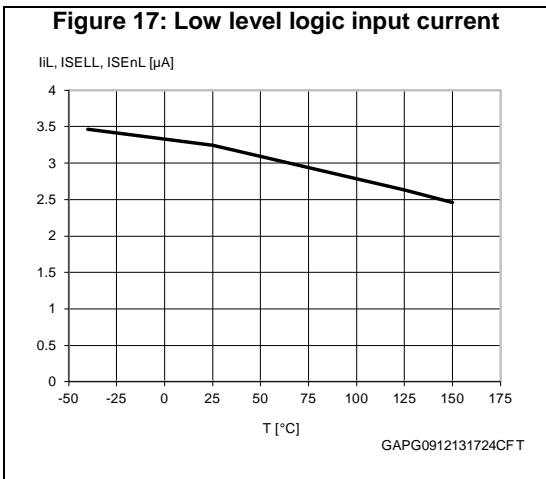
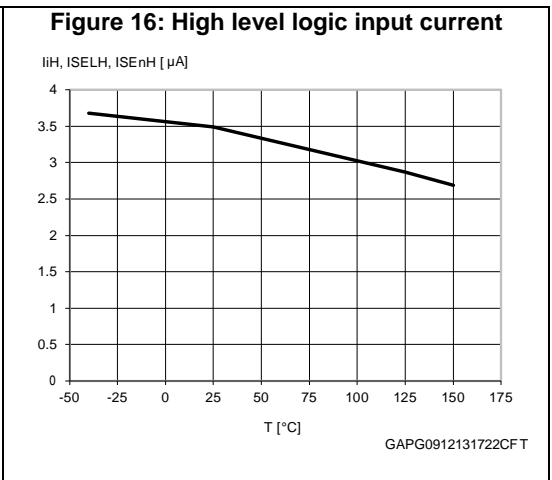
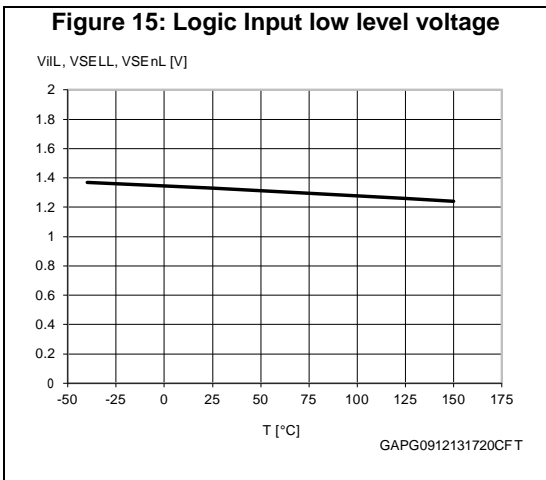
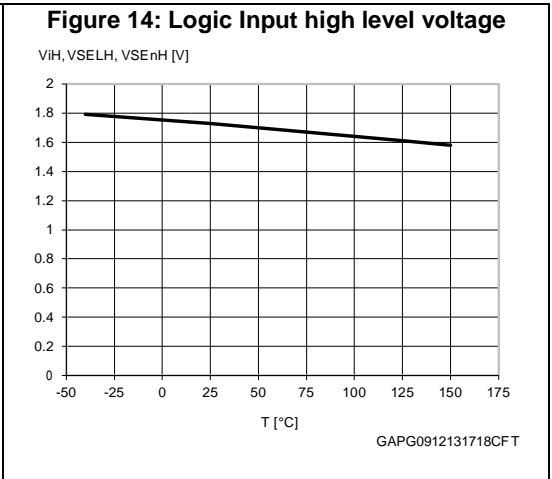
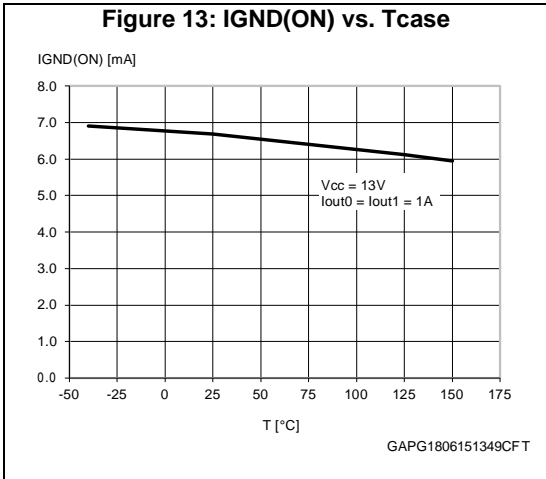


Figure 19: Undervoltage shutdown

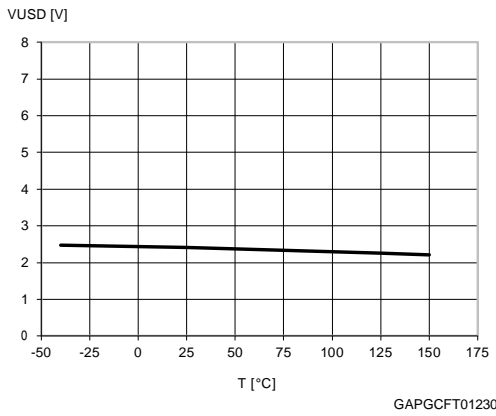


Figure 20: On-state resistance vs. Tcase

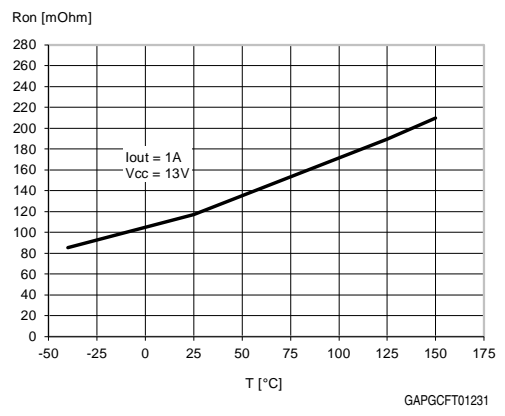


Figure 21: On-state resistance vs. Vcc

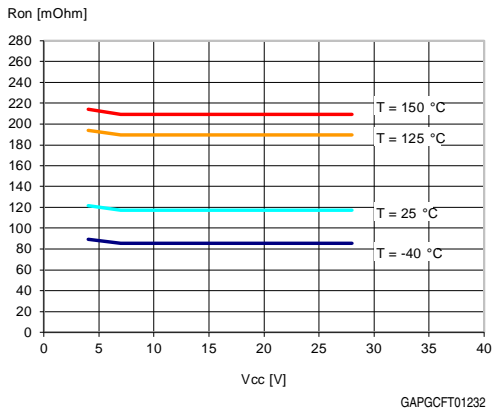


Figure 22: Turn-on voltage slope

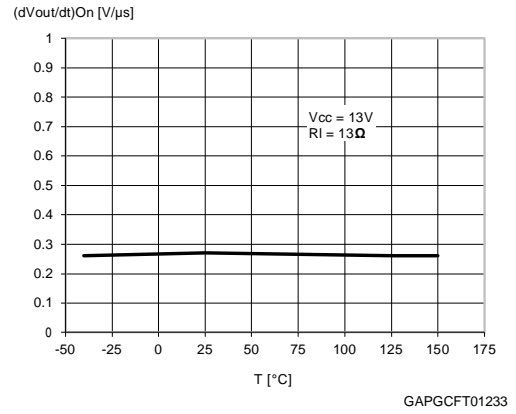


Figure 23: Turn-off voltage slope

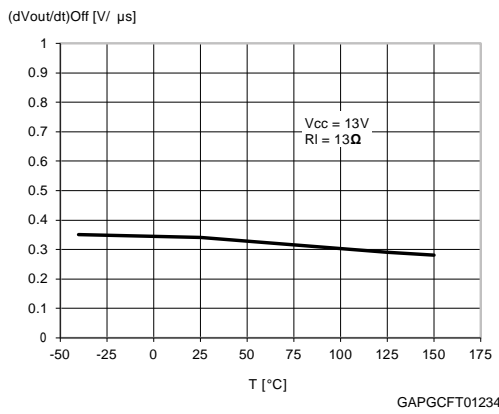
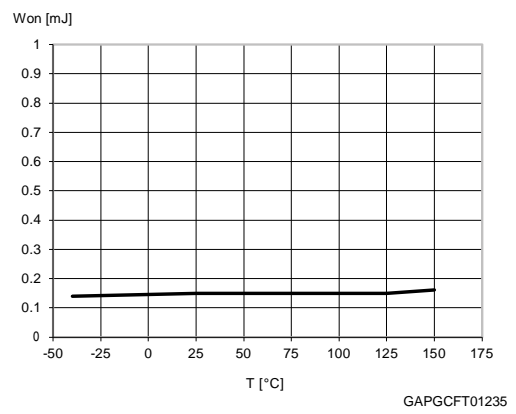
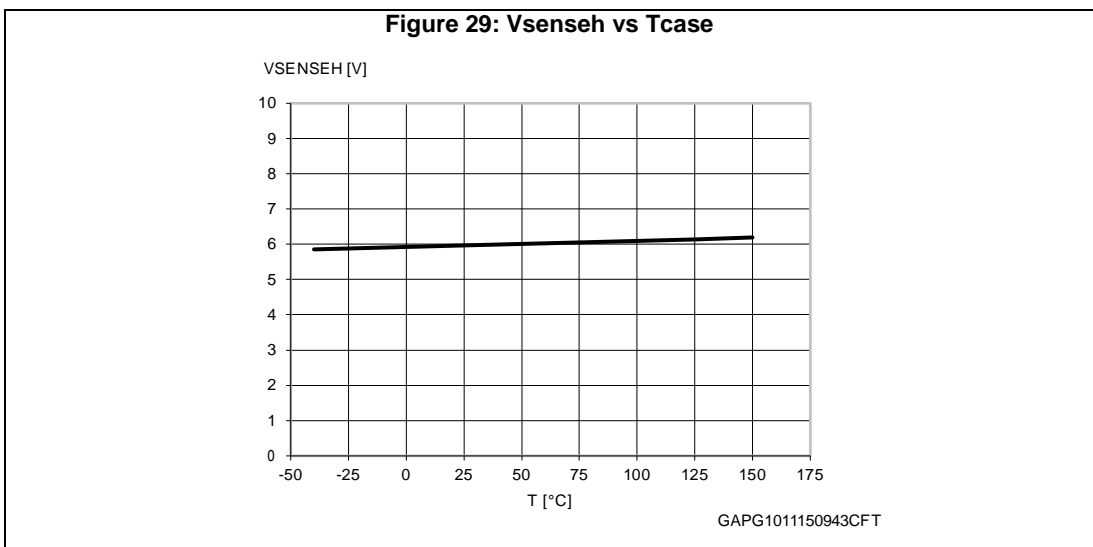
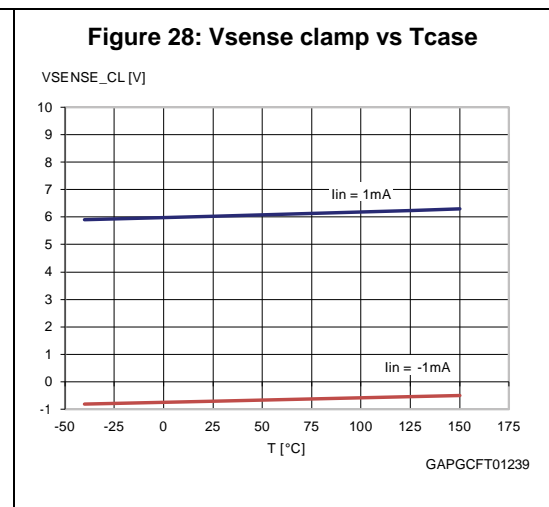
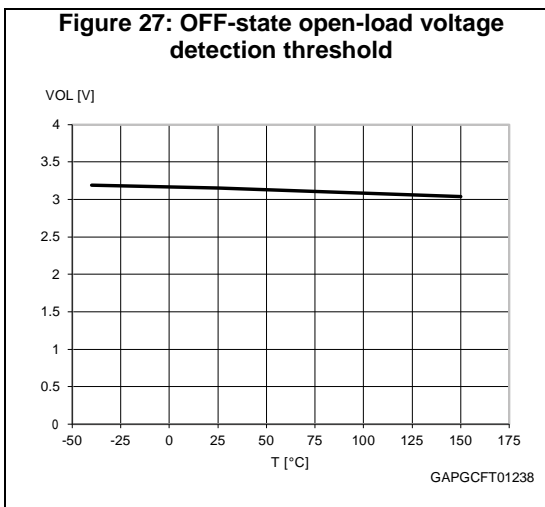
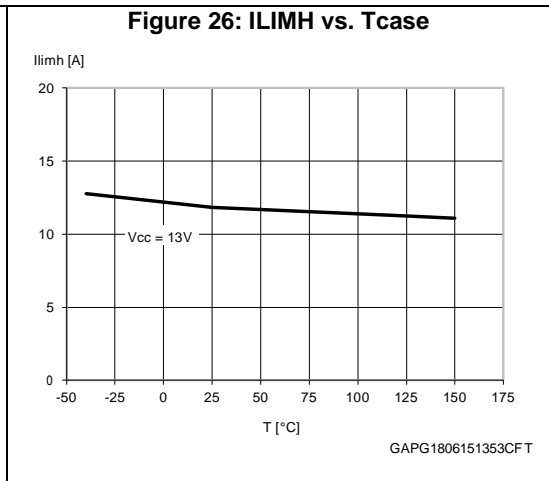
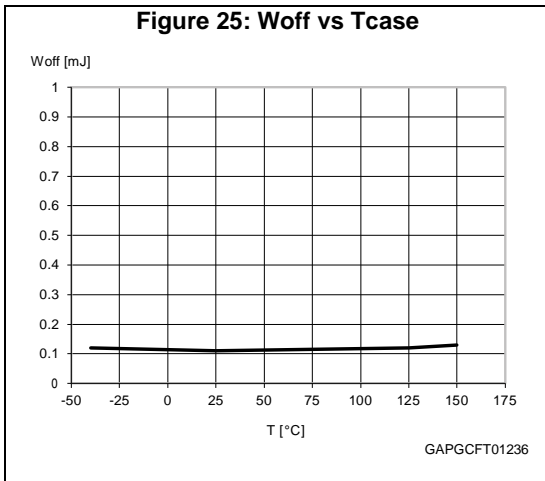


Figure 24: Won vs Tcase





3 Protections

3.1 Power limitation

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing ΔT_j through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as ΔT_j exceeds the safety level of ΔT_{j_SD} . The output MOSFET switches on and cycles with a thermal hysteresis according to the maximum instantaneous power which can be handled. The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue.

3.2 Thermal shutdown

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 175°C), it automatically switches off and the diagnostic indication is triggered. The device switches on again as soon as its junction temperature drops to T_R .

3.3 Current limitation

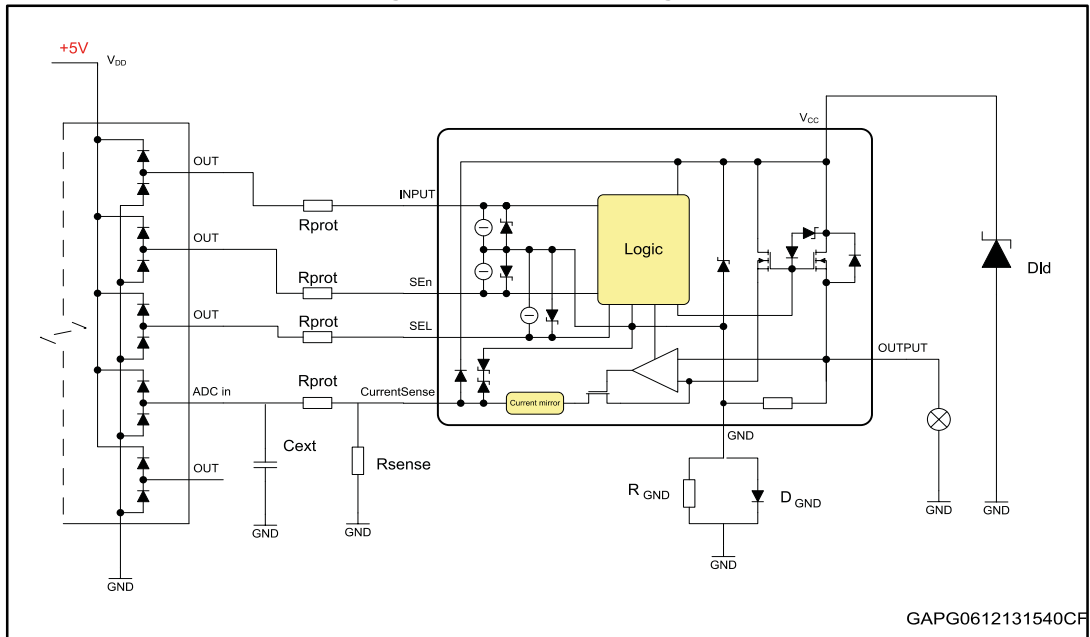
The device is equipped with an output current limiter in order to protect the silicon as well as the other components of the system (e.g. bonding wires, wiring harness, connectors, loads, etc.) from excessive current flow. Consequently, in case of short circuit, overload or during load power-up, the output current is clamped to a safety level, I_{LIMH} , by operating the output power MOSFET in the active region.

3.4 Negative voltage clamp

In case the device drives inductive load, the output voltage reaches a negative value during turn off. A negative voltage clamp structure limits the maximum negative voltage to a certain value, V_{DEMAG} , allowing the inductor energy to be dissipated without damaging the device.

4 Application information

Figure 30: Application diagram



4.1 GND protection network against reverse battery

Figure 31: Simplified internal structure - GND network protection with Schottly diode

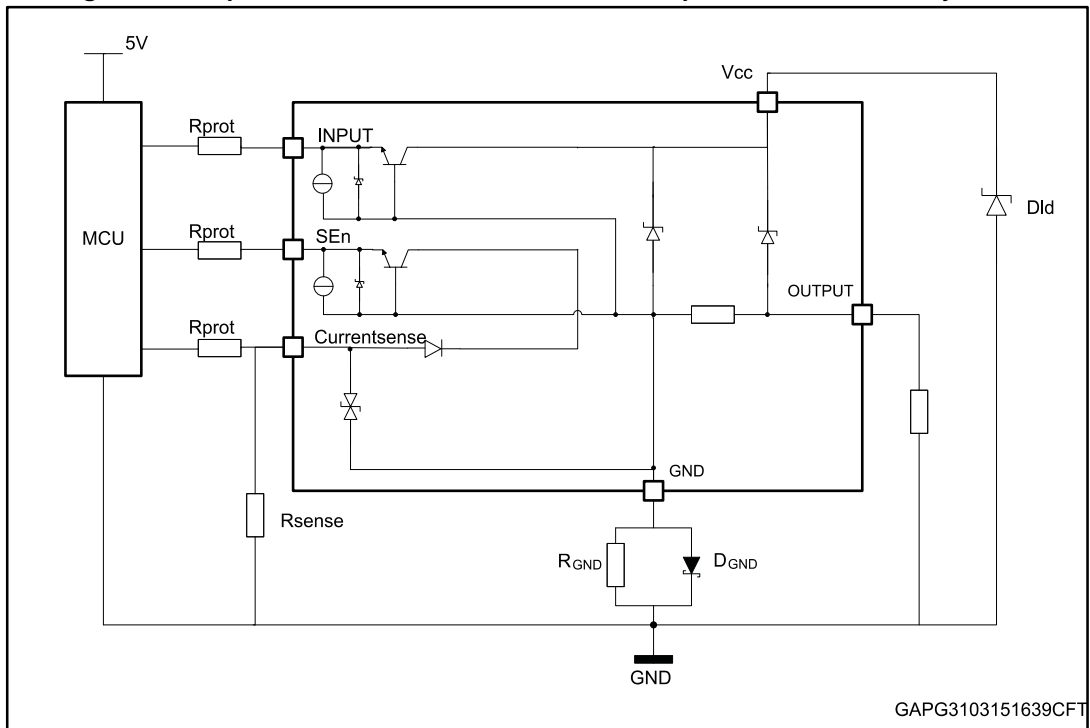
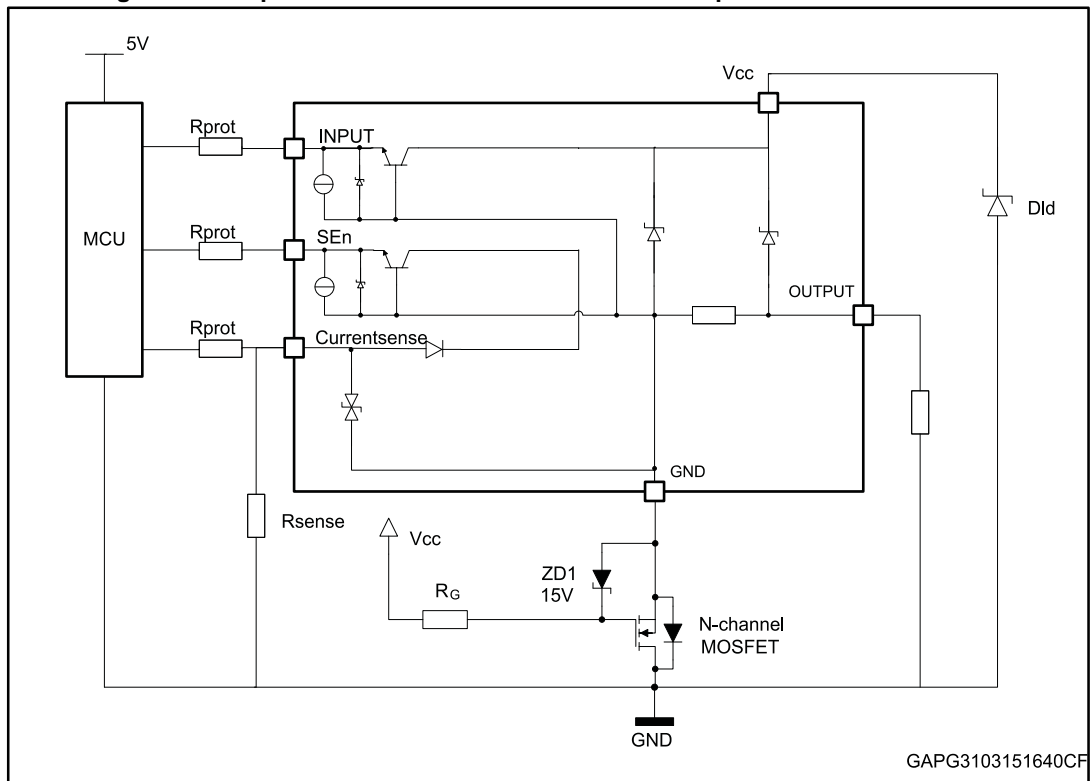


Figure 32: Simplified internal structure - GND network protection with MOSFET



4.1.1 Diode (DGND) in the ground line

A resistor (typ. $R_{GND} = 4.7 \text{ k}\Omega$) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift ($\gg 600 \text{ mV}$) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

To comply with LV124, E-11 "severe" start pulse, a Schottky diode (see [Figure 31: "Simplified internal structure - GND network protection with Schottky diode"](#)) or N-channel MOSFET (see [Figure 32: "Simplified internal structure - GND network protection with MOSFET"](#)) is recommended in order to ensure a lower ground network shift ($\leq 350 \text{ mV}$).

4.2 Immunity against transient electrical disturbances

The immunity of the device against transient electrical emissions, conducted along the supply lines and injected into the V_{CC} pin, is tested in accordance with ISO7637-2:2011 (E) and ISO 16750-2:2010.

The related function performance status classification is shown in [Table 13: "ISO 7637-2 - electrical transient conduction along supply line"](#).

Test pulses are applied directly to DUT (Device Under Test) both in ON and OFF-state and in accordance to ISO 7637-2:2011(E), chapter 4. The DUT is intended as the present device only, without components and accessed through V_{CC} and GND terminals.

Status II is defined in ISO 7637-1 Function Performance Status Classification (FPSC) as follows: "The function does not perform as designed during the test but returns automatically to normal operation after the test".

Table 13: ISO 7637-2 - electrical transient conduction along supply line

| Test Pulse 2011(E) | Test pulse severity level with Status II functional performance status | | Minimum number of pulses or test time | Burst cycle / pulse repetition time | | Pulse duration and pulse generator internal impedance |
|--|--|-------------------------------|---------------------------------------|-------------------------------------|--------|---|
| | Level | U _s ⁽¹⁾ | | min | max | |
| 1 | III | -112V | 500 pulses | 0,5 s | | 2ms, 10Ω |
| 2a | III | +55V | 500 pulses | 0,2 s | 5 s | 50μs, 2Ω |
| 3a | IV | -220V | 1h | 90 ms | 100 ms | 0.1μs, 50Ω |
| 3b | IV | +150V | 1h | 90 ms | 100 ms | 0.1μs, 50Ω |
| 4 ⁽²⁾ | IV | -7V | 1 pulse | | | 100ms, 0.01Ω |
| Load dump according to ISO 16750-2:2010 | | | | | | |
| Test B ⁽³⁾ | | 40V | 5 pulse | 1 min | | 400ms, 2Ω |

Notes:

⁽¹⁾U_s is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E), chapter 5.6.

⁽²⁾Test pulse from ISO 7637-2:2004(E).

⁽³⁾With 40 V external suppressor referred to ground (-40°C < T_j < 150°C).

4.3 MCU I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line both to prevent the microcontroller I/O pins to latch-up and to protect the HSD inputs.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation

$$V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For V_{CCpeak} = -150 V; I_{latchup} ≥ 20 mA; V_{OHμC} ≥ 4.5 V

$$7.5 \text{ k}\Omega \leq R_{prot} \leq 140 \text{ k}\Omega.$$

Recommended values: R_{prot} = 15 kΩ

4.4 Behaviour during engine start transients

The battery voltage drops every time an engine start occurs as well as in start&stop automotive systems.

The device is designed to operate during engine start pulses without external components.

In particular, the device achieves functional status A, for both E-11 start pulses, "normal" and "severe" as defined in [Table 14: "Test parameters, E-11 Start pulses"](#).

Functional status A is defined as follows: the DUT (device under test) must fulfill all functions during and after exposure to the test parameters.

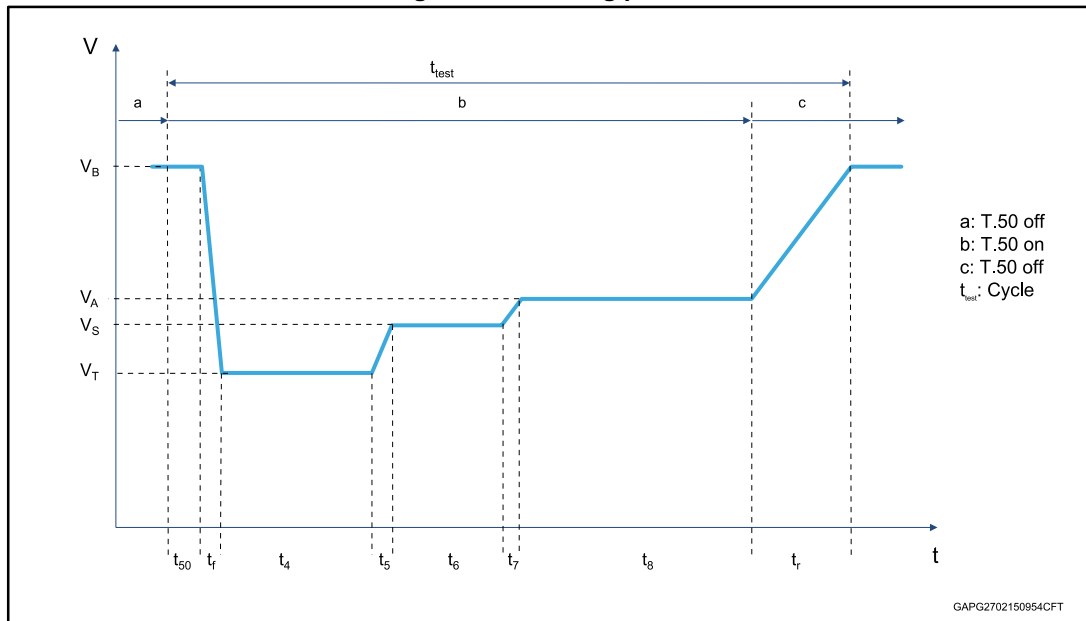
Table 14: Test parameters, E-11 Start pulses

| Parameter | Test pulse “normal” | Test pulse “severe” |
|--------------------------|---------------------|------------------------|
| V_B | 11,0 V | 11,0 V |
| V_T | 4,5 V (0%, -4%) | 3,2 V ^{+0,2V} |
| V_S | 4,5 V (0%, -4%) | 5,0 V (0%, -4%) |
| V_A | 6,5 V (0%, -4%) | 6,0 V (0%, -4%) |
| V_R | 2 V | 2 V |
| t_f | ≤1 ms | ≤1 ms |
| t_4 | 0 ms | 19 ms |
| t_5 | 0 ms | ≤1 ms |
| t_6 | 19 ms | 329 ms |
| t_7 | 50 ms | 50 ms |
| t_8 | 10 s | 10 s |
| t_r | 100 ms | 100 ms |
| f | 2 Hz | 2 Hz |
| Break between two cycles | 2 s | 2 s |
| Test cycles | 10 | 10 |



For more details see standard norm “LV124 - Electric and Electronic Components in Motor Vehicles up to 3.5 t”.

Figure 33: Cranking profile



The extremely low $V_{USD_Cranking}$, minimum cranking supply voltage (V_{CC} decreasing), specification of 2.85 V, much lower than the standard requirement, allows the device

operating in all the applications where a ground network protection is required (see [Section 4.1: "GND protection network against reverse battery"](#)).

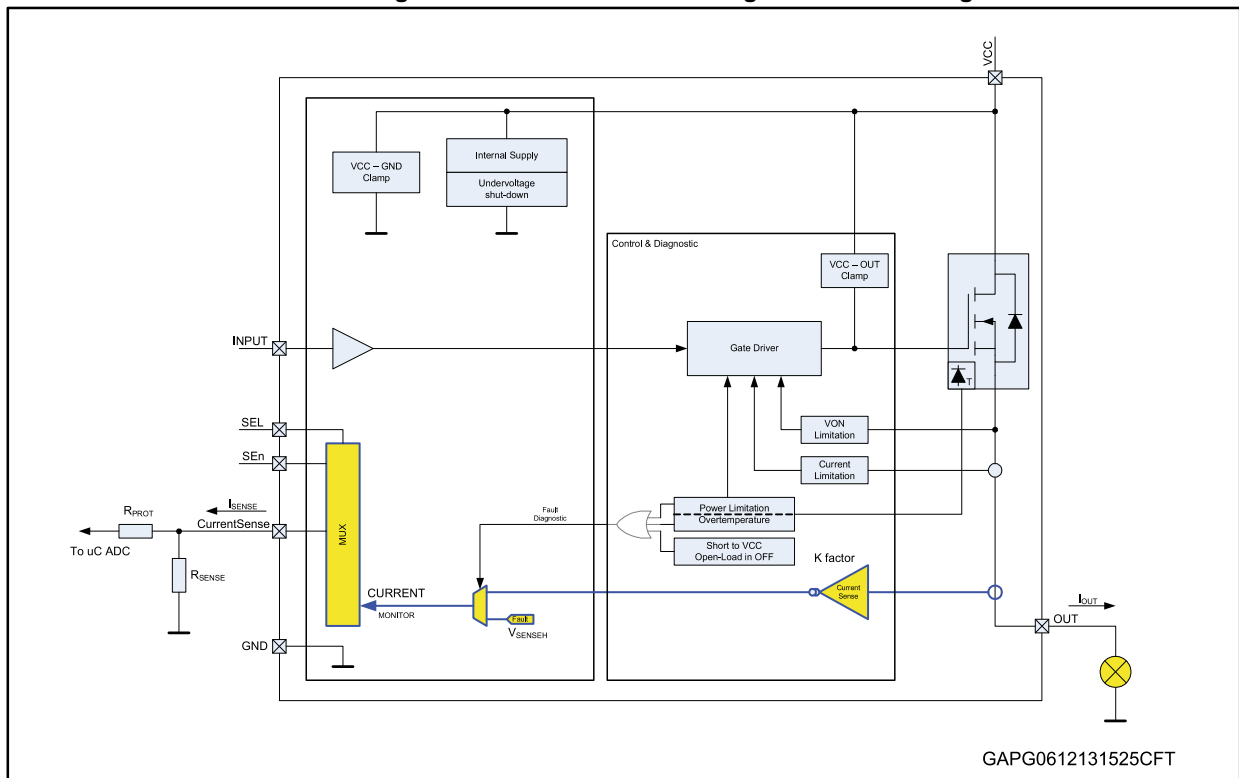
Table 15: Cranking operating mode

| Operating range | Voltage range | Operating mode |
|-----------------------------|---------------|---|
| Normal mode 4 V to 28 V | 18 V - 28 V | All functions are performed as specified. Some deviations of the electrical characteristics. |
| | 7 V - 18 V | All functions are performed as specified. All parameters in range. |
| | 4 V - 7 V | All functions are performed as specified. Some deviations of the electrical characteristics. |
| Cranking mode 2.85 V to 4 V | 2.85 V - 4 V | Device is operating (V_{CC} decreasing). Device is protected. No diagnostic. Electrical parameters deviations. |

4.5 CurrentSense - analog current sense

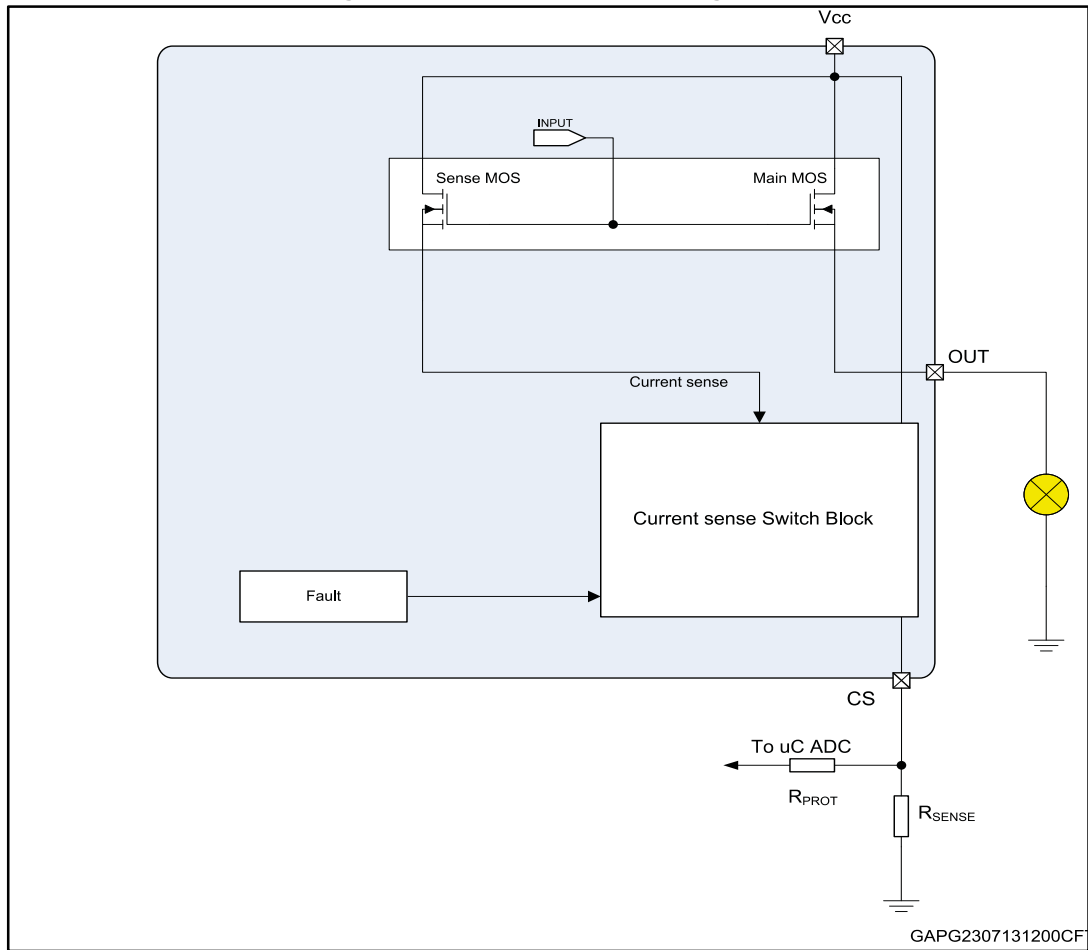
Diagnostic information on device and load status are provided by an analog output pin (CurrentSense) delivering a current mirror of channel output current

Figure 34: CurrentSense and diagnostic – block diagram



4.5.1 Principle of CurrenSense signal generation

Figure 35: CurrentSense block diagram



Current monitor

This output is capable of providing:

- **Current mirror proportional to the load current in normal operation**, delivering current proportional to the load according to known ratio named **K**
- **Diagnostics flag in fault conditions** delivering fixed voltage V_{SENSEH}

The current delivered by the current sense circuit, I_{SENSE} , can be easily converted to a voltage V_{SENSE} by using an external sense resistor, R_{SENSE} , allowing continuous load monitoring and abnormal condition detection.

Normal operation (channel ON, no fault, SEn active)

While device is operating in normal conditions (no fault intervention), V_{SENSE} calculation can be done using simple equations

Current provided by CurrentSense output: $I_{SENSE} = I_{OUT}/K$

Voltage on R_{SENSE} : $V_{SENSE} = R_{SENSE} \cdot I_{SENSE} = R_{SENSE} \cdot I_{OUT}/K$

Where :

- V_{SENSE} is voltage measurable on R_{SENSE} resistor

- I_{SENSE} is current provided from CurrentSense pin in current output mode
- I_{OUT} is current flowing through output
- K factor represents the ratio between PowerMOS cells and SenseMOS cells; its spread includes geometric factor spread, current sense amplifier offset and process parameters spread of overall circuitry specifying ratio between I_{OUT} and I_{SENSE} .

Failure flag indication

In case of power limitation/overtemperature, the fault is indicated by the CurrentSense pin which is switched to a “current limited” voltage source, V_{SENSEH} .

In any case, the current sourced by the CurrentSense in this condition is limited to I_{SENSEH} .

The typical behavior in case of overload or hard short circuit is shown in *Waveforms section*.

Figure 36: Analogue HSD – open-load detection in off-state

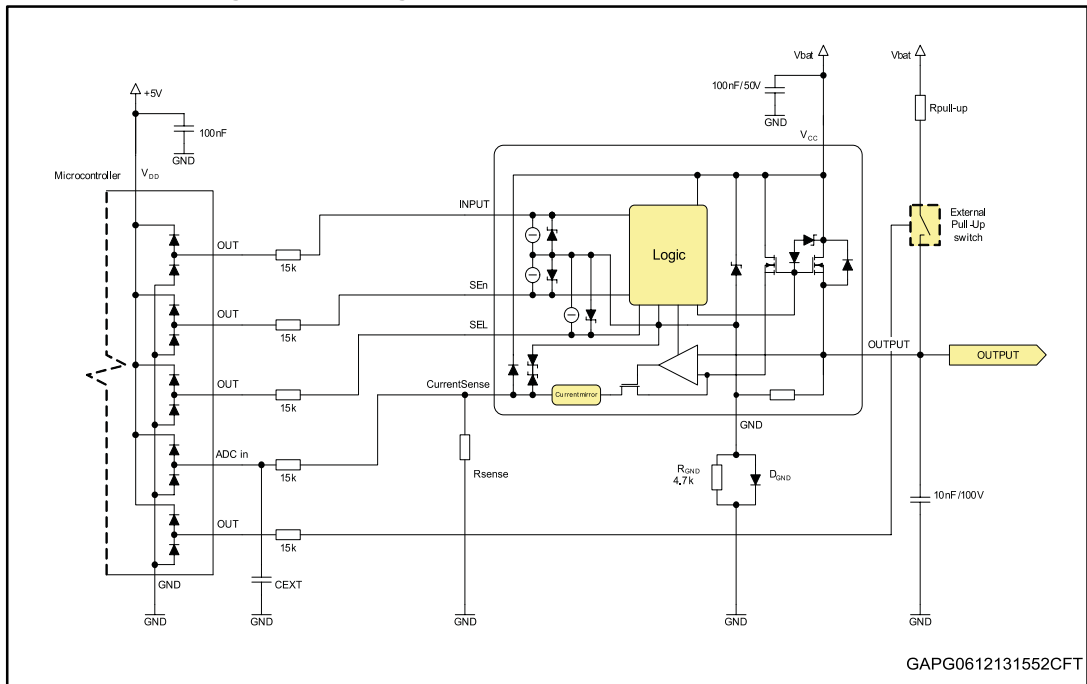


Figure 37: Open-load / short to VCC condition

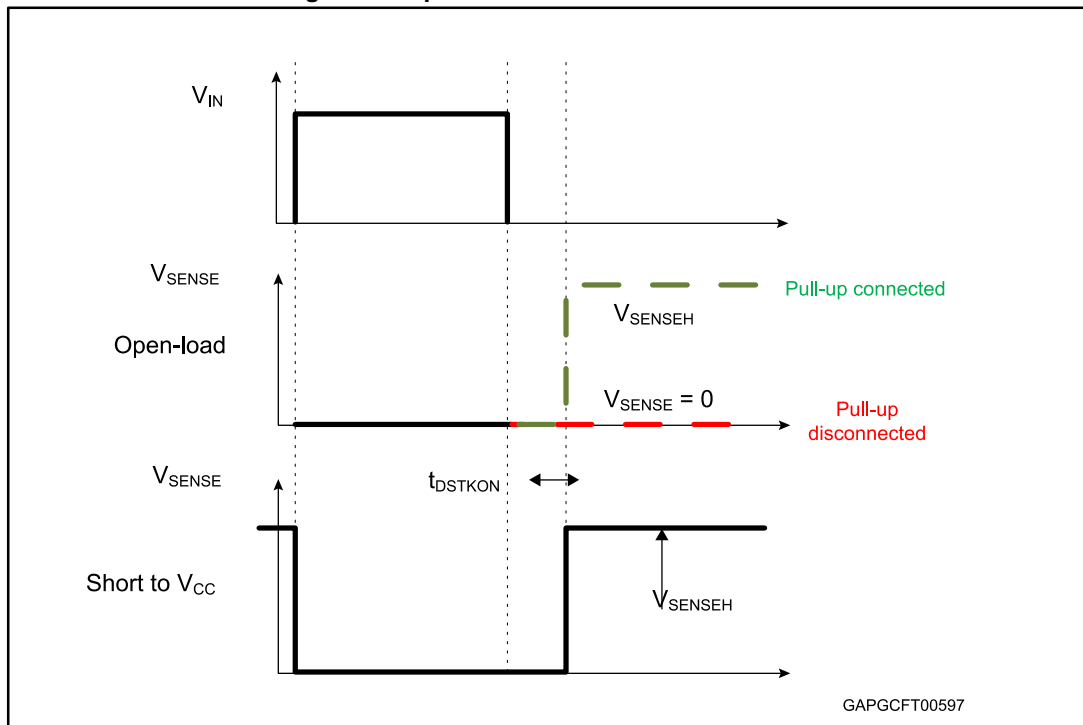


Table 16: CurrentSense pin levels in off-state

| Condition | Output | CurrentSense | SEn |
|-------------------|--------------------|--------------|-----|
| Open-load | $V_{OUT} > V_{OL}$ | Hi-Z | L |
| | | V_{SENSEH} | H |
| | $V_{OUT} < V_{OL}$ | Hi-Z | L |
| | | 0 | H |
| Short to V_{CC} | $V_{OUT} > V_{OL}$ | Hi-Z | L |
| | | V_{SENSEH} | H |
| Nominal | $V_{OUT} < V_{OL}$ | Hi-Z | L |
| | | 0 | H |

4.5.2 Short to VCC and OFF-state open-load detection

Short to V_{CC}

A short circuit between V_{CC} and output is indicated by the relevant current sense pin set to V_{SENSEH} during the device off-state. Small or no current is delivered by the current sense during the on-state depending on the nature of the short circuit.

OFF-state open-load with external circuitry

Detection of an open-load in off mode requires an external pull-up resistor R_{PU} connecting the output to a positive supply voltage V_{PU} .

It is preferable V_{PU} to be switched off during the module standby mode in order to avoid the overall standby current consumption to increase in normal conditions, i.e. when load is connected.

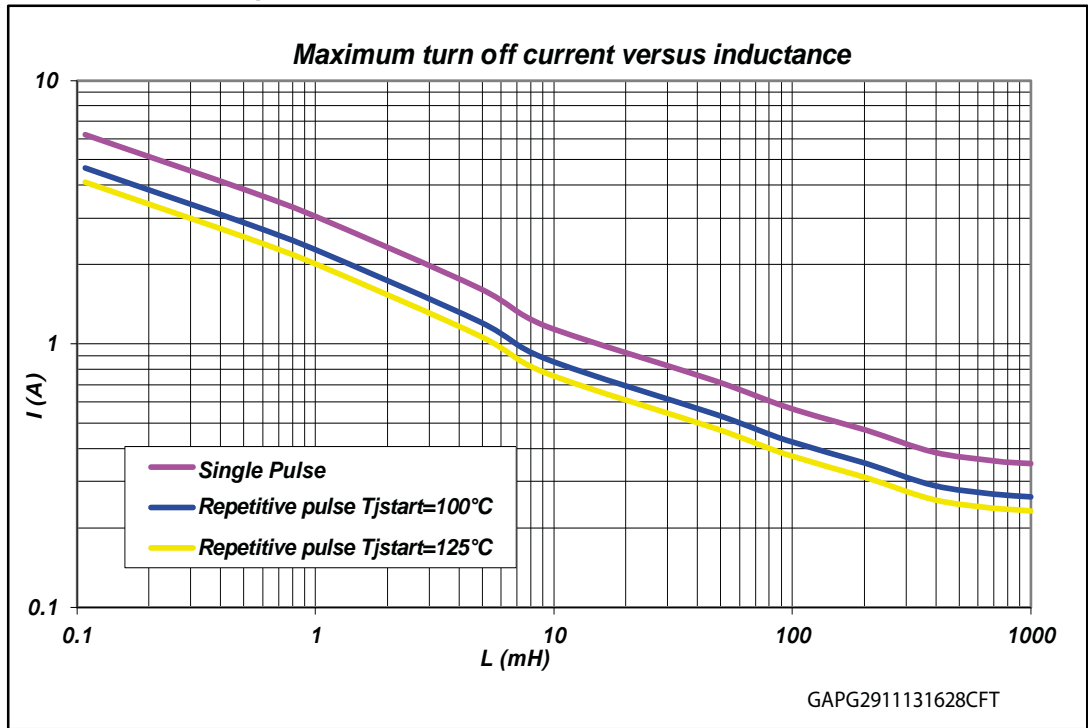
R_{PU} must be selected in order to ensure $V_{OUT} > V_{OLmax}$ in accordance with the following equation:

Equation

$$R_{PU} < \frac{V_{PU} - 4}{I_{L(off2)min @ 4V}}$$

5 Maximum demagnetization energy (VCC = 16 V)

Figure 38: Maximum turn off current versus inductance



Values are generated with $R_L = 0 \Omega$.

In case of repetitive pulses, T_{jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

6 Package and PCB thermal data

6.1 PowerSSO-12 thermal data

Figure 39: PowerSSO-12 on two-layers PCB (2s0p to JEDEC JESD 51-5)

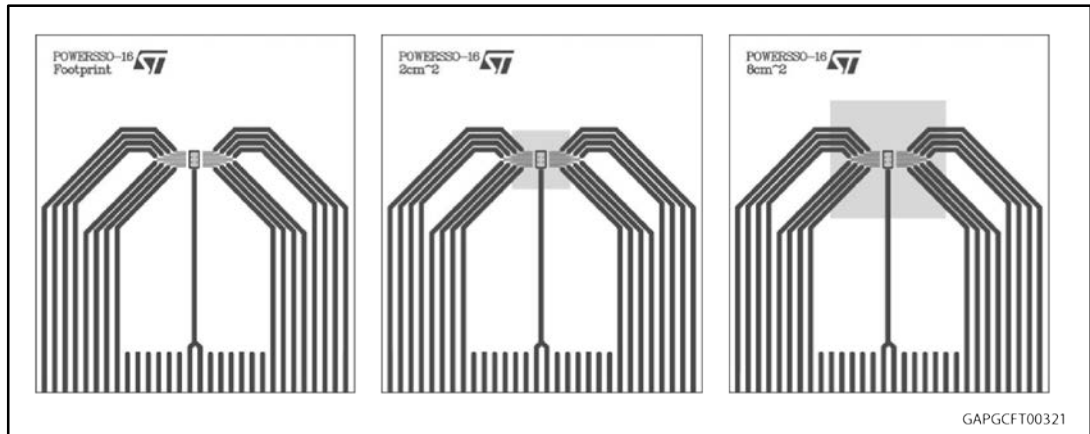


Figure 40: PowerSSO-12 on four-layers PCB (2s2p to JEDEC JESD 51-7)

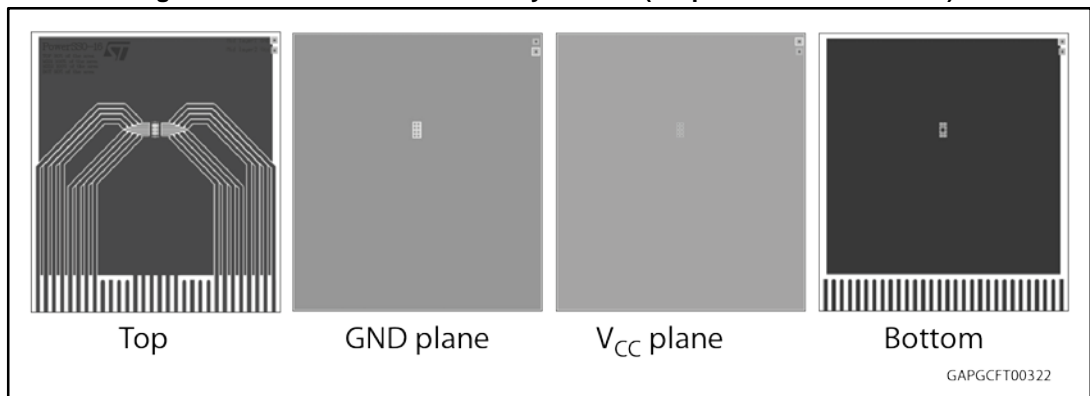


Table 17: PCB properties

| Dimension | Value |
|---|---|
| Board finish thickness | 1.6 mm +/- 10% |
| Board dimension | 77 mm x 86 mm |
| Board material | FR4 |
| Copper thickness (top and bottom layers) | 0.070 mm |
| Copper thickness (inner layers) | 0.035 mm |
| Thermal via separation | 1.2 mm |
| Thermal via diameter | 0.3 mm +/- 0.08 mm |
| Copper thickness on via | 0.025 mm |
| Footprint dimension (top layer) | 2.2 mm x 3.9 mm |
| Heatsink copper area dimension (bottom layer) | Footprint, 2 cm ² or 8 cm ² |

Figure 41: Rthj-amb vs PCB copper area in open box free air condition (one channel on)

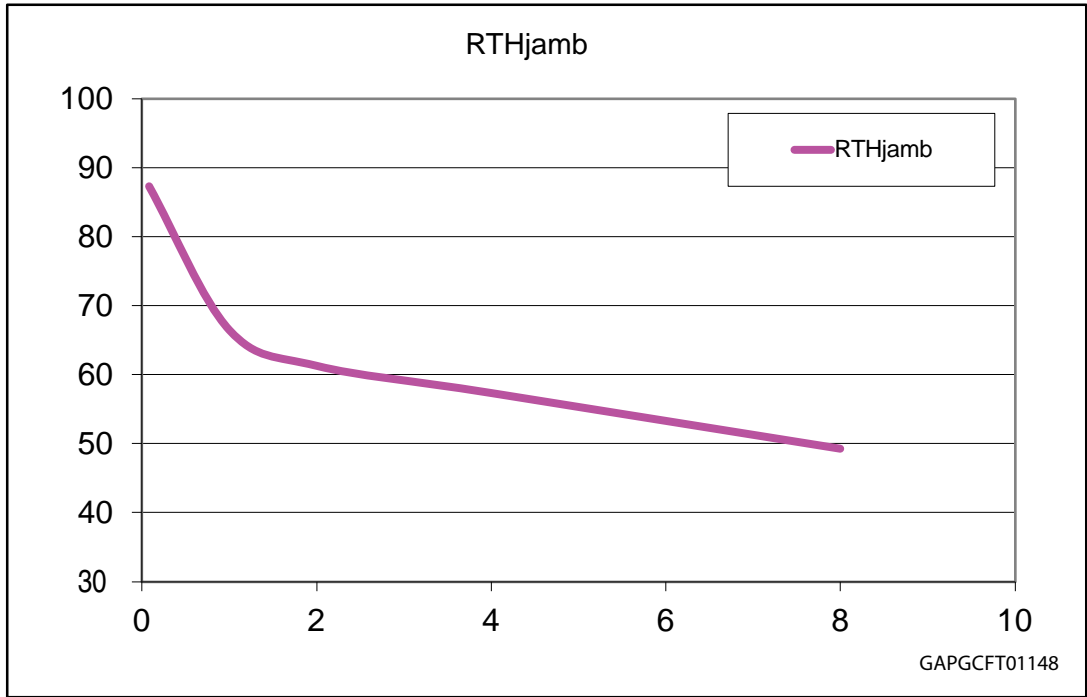
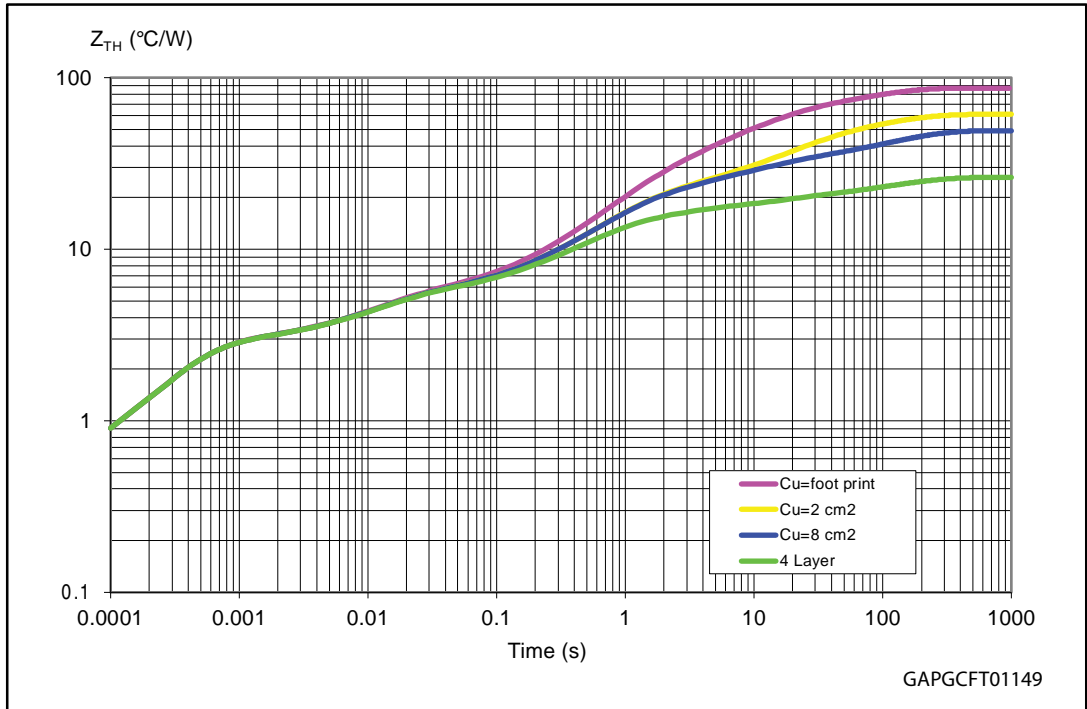


Figure 42: PowerSSO-12 thermal impedance junction ambient single pulse (one channel on)

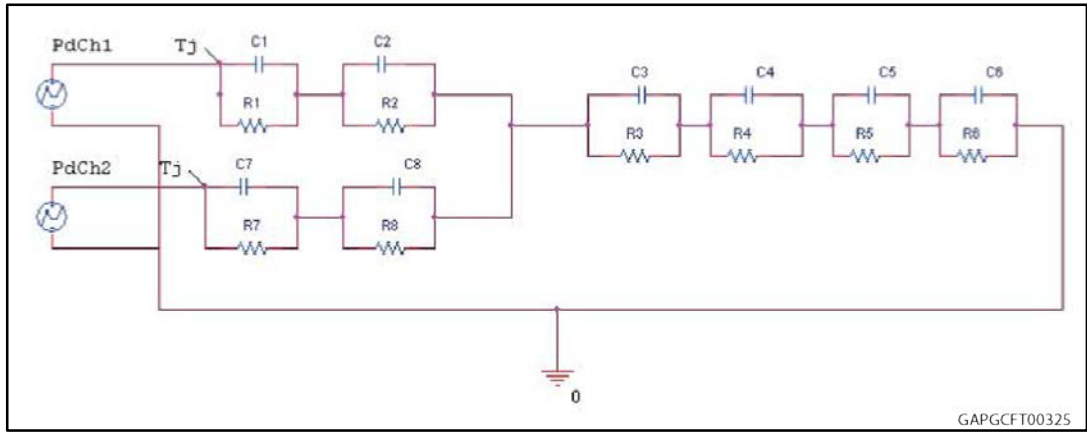


Equation: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp} (1 - \delta)$$

where $\delta = t_p/T$

Figure 43: Thermal fitting model of a double-channel HSD in PowerSSO-12



The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 18: Thermal parameters

| Area/island (cm ²) | Footprint | 2 | 8 | 4L |
|--------------------------------|-----------|-----|-----|-----|
| R1 = R7 (°C/W) | 2.8 | | | |
| R2 = R8 (°C/W) | 2.5 | | | |
| R3 (°C/W) | 10 | 10 | 10 | 7 |
| R4 (°C/W) | 16 | 6 | 6 | 4 |
| R5 (°C/W) | 30 | 20 | 10 | 3 |
| R6 (°C/W) | 26 | 20 | 18 | 7 |
| C1 = C7 (W.s/°C) | 0.00012 | | | |
| C2 = C8 (W.s/°C) | 0.005 | | | |
| C3 (W.s/°C) | 0.07 | | | |
| C4 (W.s/°C) | 0.2 | 0.3 | 0.3 | 0.4 |
| C5 (W.s/°C) | 0.4 | 1 | 1 | 4 |
| C6 (W.s/°C) | 3 | 5 | 7 | 18 |

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

7.1 PowerSSO-12 package information

Figure 44: PowerSSO-12 package dimensions

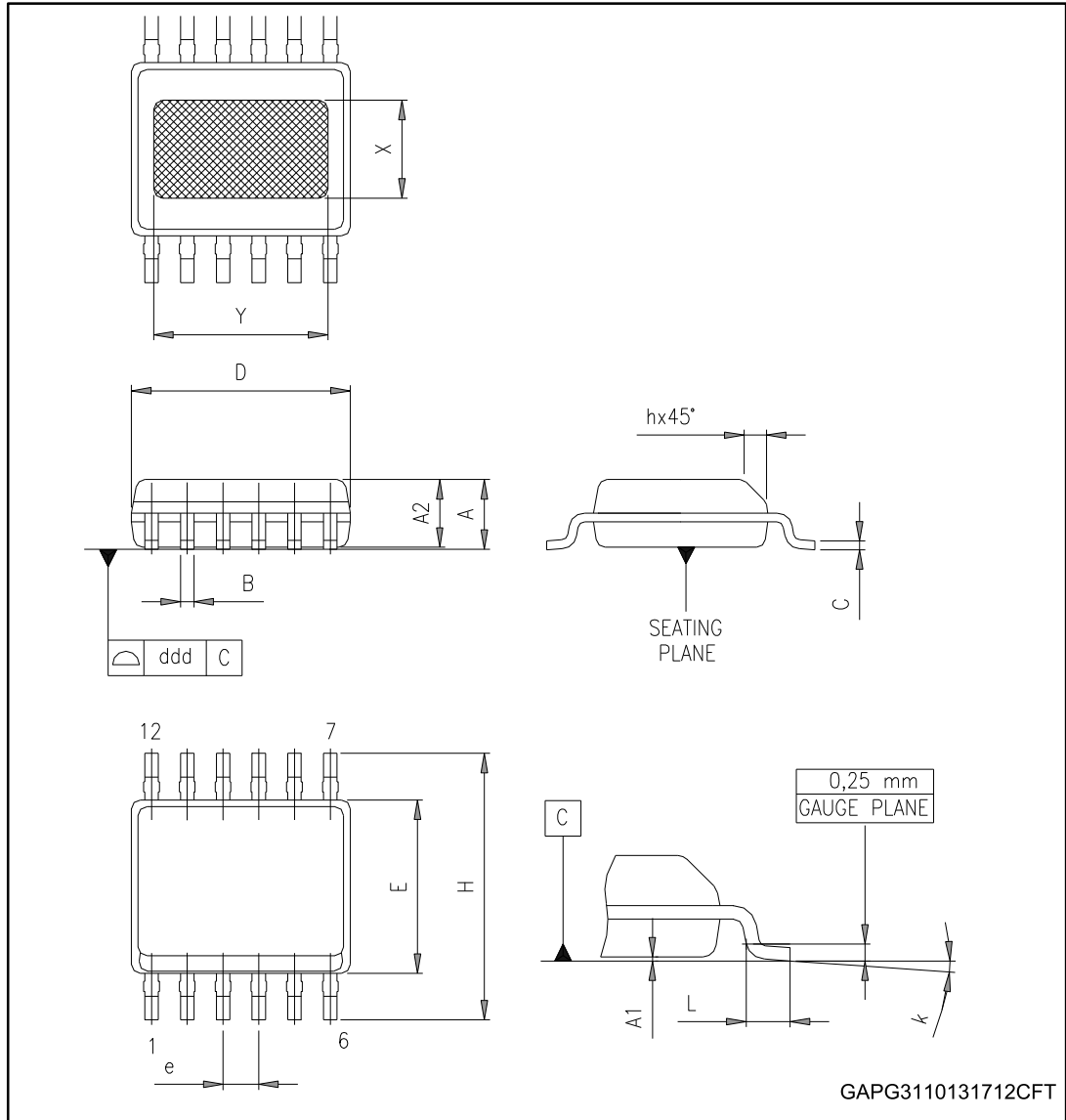


Table 19: PowerSSO-12 mechanical data

| Symbol | Millimeters | | |
|--------|-------------|-------|-------|
| | Min. | Typ. | Max. |
| A | 1.250 | | 1.700 |
| A1 | 0.000 | | 0.100 |
| A2 | 1.100 | | 1.600 |
| B | 0.230 | | 0.410 |
| C | 0.190 | | 0.250 |
| D | 4.800 | | 5.000 |
| E | 3.800 | | 4.000 |
| e | | 0.800 | |
| H | 5.800 | | 6.200 |
| h | 0.250 | | 0.500 |
| L | 0.400 | | 1.270 |
| k | 0° | | 8° |
| X | 2.200 | | 2.800 |
| Y | 2.900 | | 3.500 |
| ddd | | | 0.100 |

7.2 PowerSSO-12 packing information

Figure 45: PowerSSO-12 reel 13"

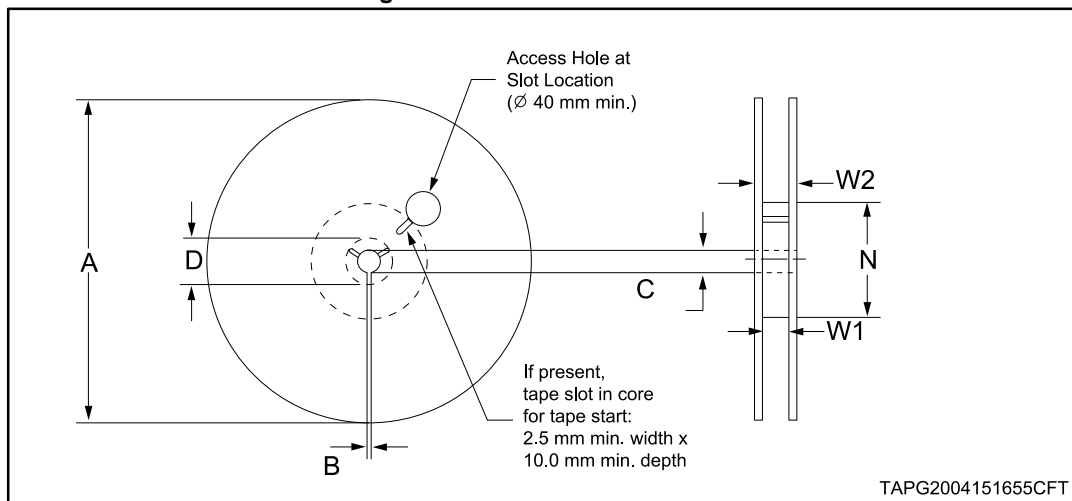


Table 20: Reel dimensions

| Description | Value ⁽¹⁾ |
|---------------|----------------------|
| Base quantity | 2500 |
| Bulk quantity | 2500 |
| A (max) | 330 |
| B (min) | 1.5 |

| Description | Value ⁽¹⁾ |
|----------------|----------------------|
| C (+0.5, -0.2) | 13 |
| D (min) | 20.2 |
| N | 100 |
| W1 (+2 /-0) | 12.4 |
| W2 (max) | 18.4 |

Notes:

(1)All dimensions are in mm.

Figure 46: PowerSSO-12 carrier tape

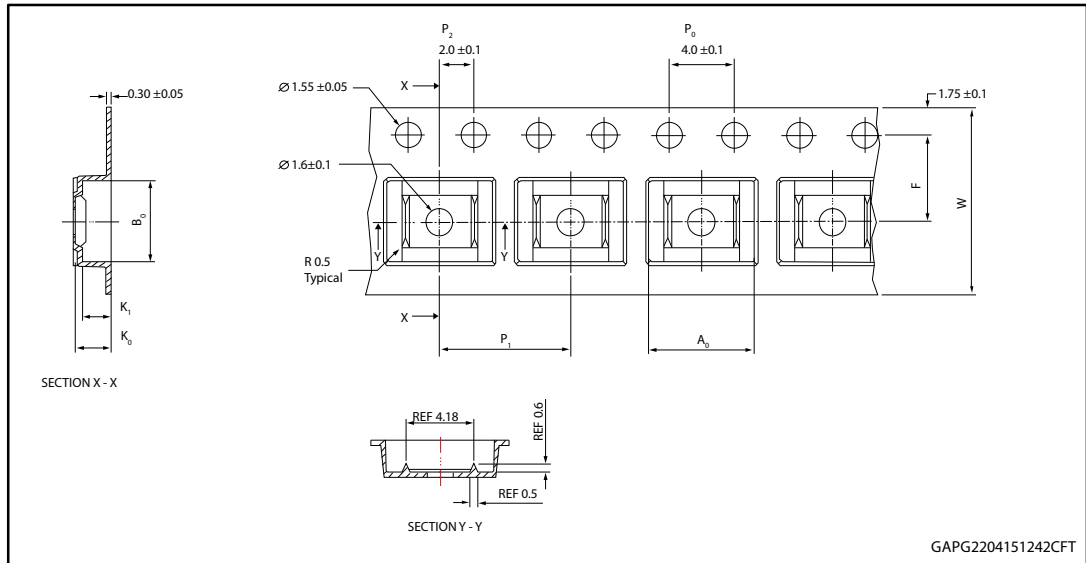


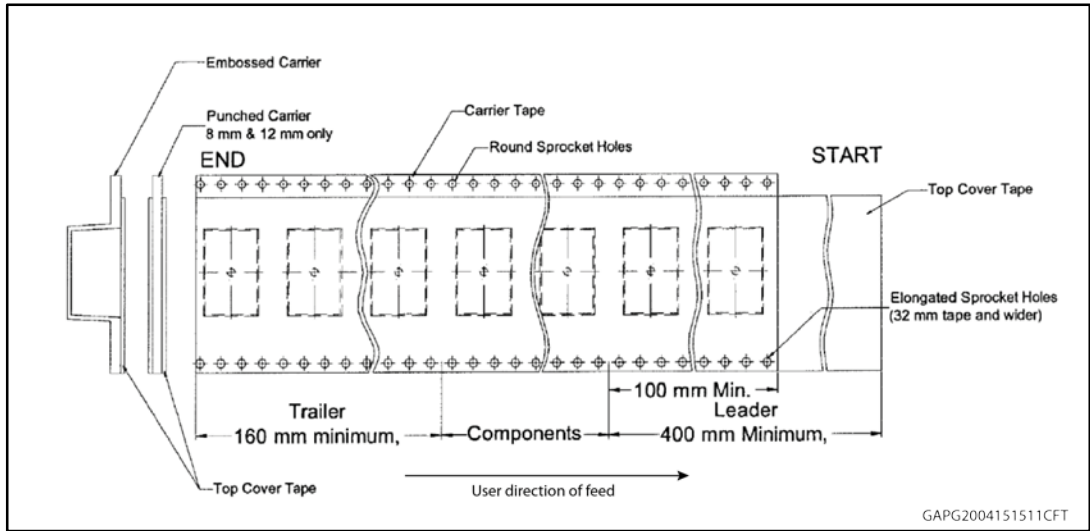
Table 21: PowerSSO-12 carrier tape dimensions

| Description | Value ⁽¹⁾ |
|-------------|----------------------|
| A_0 | 6.50 ± 0.1 |
| B_0 | 5.25 ± 0.1 |
| K_0 | 2.10 ± 0.1 |
| K_1 | 1.80 ± 0.1 |
| F | 5.50 ± 0.1 |
| P_1 | 8.00 ± 0.1 |
| W | 12.00 ± 0.3 |

Notes:

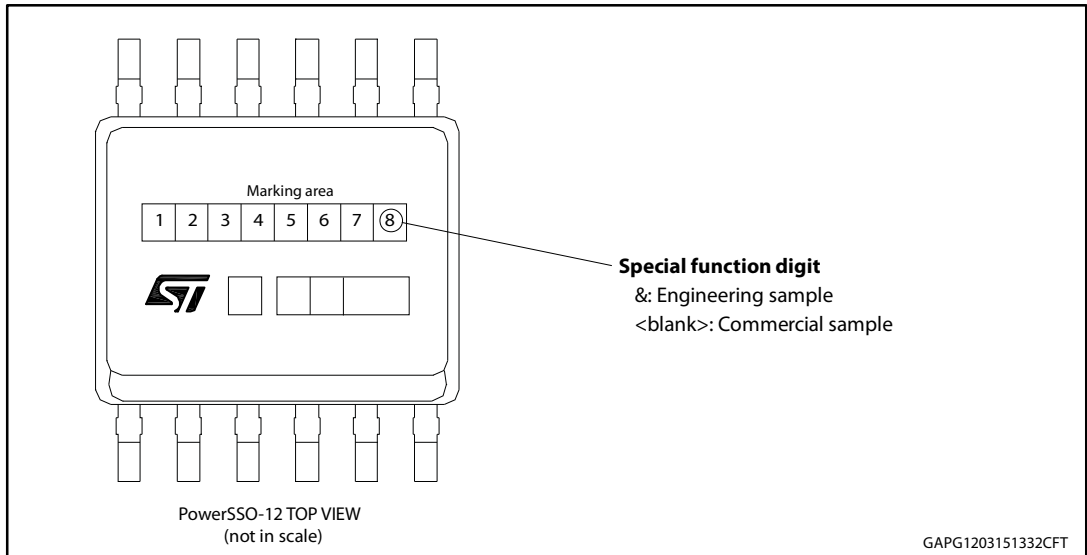
(1)All dimensions are in mm.

Figure 47: PowerSSO-12 schematic drawing of leader and trailer tape



7.3 PowerSSO-12 marking information

Figure 48: PowerSSO-12 marking information



Engineering Samples: these samples can be clearly identified by a dedicated special symbol in the marking of each unit. These samples are intended to be used for electrical compatibility evaluation only; usage for any other purpose may be agreed only upon written authorization by ST. ST is not liable for any customer usage in production and/or in reliability qualification trials.

Commercial Samples: Fully qualified parts from ST standard production with no usage restrictions

8 Order codes

Table 22: Device summary

| Package | Order codes |
|-------------|---------------|
| | Tape and reel |
| PowerSSO-12 | VND7140AJ12TR |

9 Revision history

Table 23: Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 09-Jun-2015 | 1 | Initial release. |
| 18-Jun-2015 | 2 | <i>Table 5: "Electrical characteristics during cranking":</i> <ul style="list-style-type: none">• T_{TSD}: updated value <i>Table 10: "CurrentSense":</i> <ul style="list-style-type: none">• K_{OL}, K_{LED}, K_0, K_1: updated values Updated <i>Section 2.5: "Electrical characteristics curves"</i> |
| 14-Sep-2015 | 3 | Updated <i>Table 1: "Pin functions"</i> <i>Table 5: "Electrical characteristics during cranking":</i> <ul style="list-style-type: none">• R_{ON}: updated test conditions |

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