8-Bit MCU
C8051F85x/86x Errata

This document contains information on the C8051F85x/86x errata. The latest available revision of this device is revision C.

For errata on older revisions, refer to the errata history section for the device. The revision information is typically specified in or near the trace code on the device. Refer to the package marking information in the data sheet for more information.

Errata effective date: October, 2018.

1. Active Errata Summary

These tables list all known errata for the C8051F85x/86x and all unresolved errata in revision C of the C8051F85x/86x.

Table 1.1. Errata History Overview

Designator	Title/Problem	Exists on Revision:		
		A	B	C
PKG_E103	Extended Temperature Devices in Engineering Status	X	X	X
UID_E101	Unique Identifier	—	—	X
WDT_E101	Restrictions on Watchdog Timer Refresh Interval	X	X	X
WDT_E102	Restrictions on changing Watchdog Timer Interval	X	X	X

Table 1.2. Active Errata Status Summary

Errata #	Designator	Title/Problem	Workaround Exists	Affected Revision	Resolution
1	WDT_E101	Restrictions on Watchdog Timer Refresh Interval	Yes	C	—
2	WDT_E102	Restrictions on changing Watchdog Timer Interval	Yes	C	—

2. Detailed Errata Descriptions

2.1 WDT_E101 – Restrictions on Watchdog Timer Refresh Interval

Description of Errata

If the Watchdog Timer (WDT) is enabled, firmware will periodically write an 0xA5 value to the WDTCN register to refresh the timer and prevent the watchdog reset from occurring. However, if firmware writes to WDTCN more than once during the same LFOSC0 clock period, the refresh signal may be canceled, resulting in an unintended watchdog reset when the timer expires.

Affected Conditions / Impacts

If firmware refreshes the watchdog more than once in the same LFOSC0 clock period, an unexpected watchdog reset can occur.

Workaround

Systems using the Watchdog Timer (WDT) should ensure that the WDT is refreshed no more than once per LFOSC0 clock period.

Firmware can do this by using timers to count LFOSC0 clock periods. There are three methods to accomplish this:

1. If Timer 3 is not already in use, set it up to capture on the LFOSC0 clock. In this mode, the value of the Timer 3 reload registers does not matter. Instead, the WDT refresh function should check for the 16-bit timer flag (TF3H) to be set in the reset watchdog function, which indicates that a capture event occurred. If the device has another timer that can capture on the LFOSC0 clock, then that timer may be used instead of Timer 3.

```
void refresh_wdt()
{
   // Only refresh if TF3H is set
   if (TMR3CN0 & (0x80))
   {
      WDTCN = 0xA5;
      TMR3CN0 &= ~(0x80);
   }
}
```

2. If any timer is already in use, is clocked from the LFOSC0, and the low overflow flag is not already in use, firmware can check the low byte overflow flag (TFnL) to ensure at least one clock period has passed. For example, using Timer 3:

```
void init_wdt()
{
  // whatever code needed to initialized watchdog

  // intentionally set the TF3L flag (assuming SFRPAGE is correct)
  TMR3CN0 |= 0x40;
}

void refresh_wdt()
{
  static uint8_t last_tmr3l = 0;

  if ( (TMR3CN0 & 0x40) || (last_tmr3l != TMR3L) )
  {
    WDTCN = 0xA5;
    TMR3CN0 &= ~0x40;
    last_tmr3l = TMR3L;
  }
}
```

3. If the application already has an accurate and reliable time base, use that timer to establish a minimum WDT refresh interval that is longer than one LFOSC0 clock period in duration, similar to method (2) above as appropriate.

See the Knowledge Base article on this errata for more information, including examples of these firmware workarounds: https://www.silabs.com/community/mcu/8-bit/knowledge-base.entry.html/2016/11/28/wdt_e101_-_restricti-Vqe5.

Note: The LFOSC0 does not halt while debugging. This can cause the timer overflow flag to be set more quickly than expected when debugging the watchdog refresh function.

Resolution

There is currently no resolution for this issue.

2.2 WDT_E102 – Restrictions on changing Watchdog Timer Interval

Description of Errata

A watchdog reset can occur when the Watchdog Timer (WDT) is disabled.

Affected Conditions / Impacts

If the WDT timeout interval is changed from a higher interval to a lower interval, regardless if the WDT is enabled or disabled, a watchdog reset can occur

Workaround

This can be resolved by refreshing and disabling the WDT before changing the WDT timeout interval from a higher interval to lower interval. Following is the sequence of code that needs to be followed when changing the WDT interval.

```
void change_interval()
{
   WDTCN = 0xA5;          // Refresh WDT
   // Insert code to wait for 2 divided LFOSC0 clock periods
   WDTCN = 0xDE;          // Disable WDT (first key)
   WDTCN = 0xAD;          // Disable WDT (second key)
   // Insert code to wait for 3 divided LFOSC0 clock periods
   WDTCN = WDT_interval   // Change the current WDT interval to a lower interval with the MSB cleared to 0
   // Insert code to wait for 1 SYSCLK clock period
}
```

Note: User must insert the code to wait. It is not explicity added in the above sequence as it depends on the divided LFOSC0 clock and the SYSCLK clock selected by the user.

Resolution

There is currently no resolution for this issue.

3. Errata History

This section contains the errata history for C8051F85x/86x devices.

For errata on latest revision, refer to the beginning of this document. The device data sheet explains how to identify chip revision, either from package marking or electronically.

3.1 Errata History Summary

This table lists all resolved errata for the C8051F85x/86x.

Table 3.1. Errata History Status Summary

Errata #	Designator	Title/Problem	Workaround Exists	Affected Revision	Resolution
1	UID_E101	Unique Identifier	No	C	C date code 1340 or later
2	PKG_E103	Extended Temperature Devices in Engineering Status	No	C	—

3.2 Detailed Errata Descriptions

3.2.1 UID_E101 – Unique Identifier

Description of Errata
Revision C devices released before date code 1340 do not implement the Unique Identifier (UID) described in data sheet revisions greater than or equal to 0.7. A four-digit assembly build date code is marked on each part on the bottom-most line. This is in the format YYWW, where YY is the two-digit assembly build calendar year and WW is the two-digit assembly build work week. All parts that have an assembly date code of 1340 or later (year 2013, work week 40) implement the unique identifier.
Affected Conditions / Impacts
Firmware will not be able to use the UID on Revision C devices with a date code prior to 1340.
Workaround
There is no workaround for this issue.
Resolution
This issue is resolved in devices with a date code of 1340 or later (year 2013, work week 40).

3.2.2 PKG_E103 – Extended Temperature Devices in Engineering Status

Description of Errata
The –I devices (-40 °C to +125 °C) are in preliminary engineering status and sampling with –G device package markings, whereas the –G devices (-40 °C to +85 °C) are in full production status. This distinction is not documented in the device data sheet. The –I devices will enter full production status by the end of Q1 2014.
Affected Conditions / Impacts
Since the qualification of the –I devices is in progress, some data sheet parameters may change upon completion of the qualification. The package marking for the –I device will be corrected prior to full production status.
Workaround
There is currently no workaround for this issue.
Resolution
The –I devices will enter full production status by the end of Q1 2014.

4. Revision History

Revision 0.3

Noivember, 2018

- Merged errata history and errata into one document.
- Updated the second workaround in WDT_E101.
- Updated Knowledge Base article link in WDT_E101.
- Added WDT_E102.

Revision 0.2

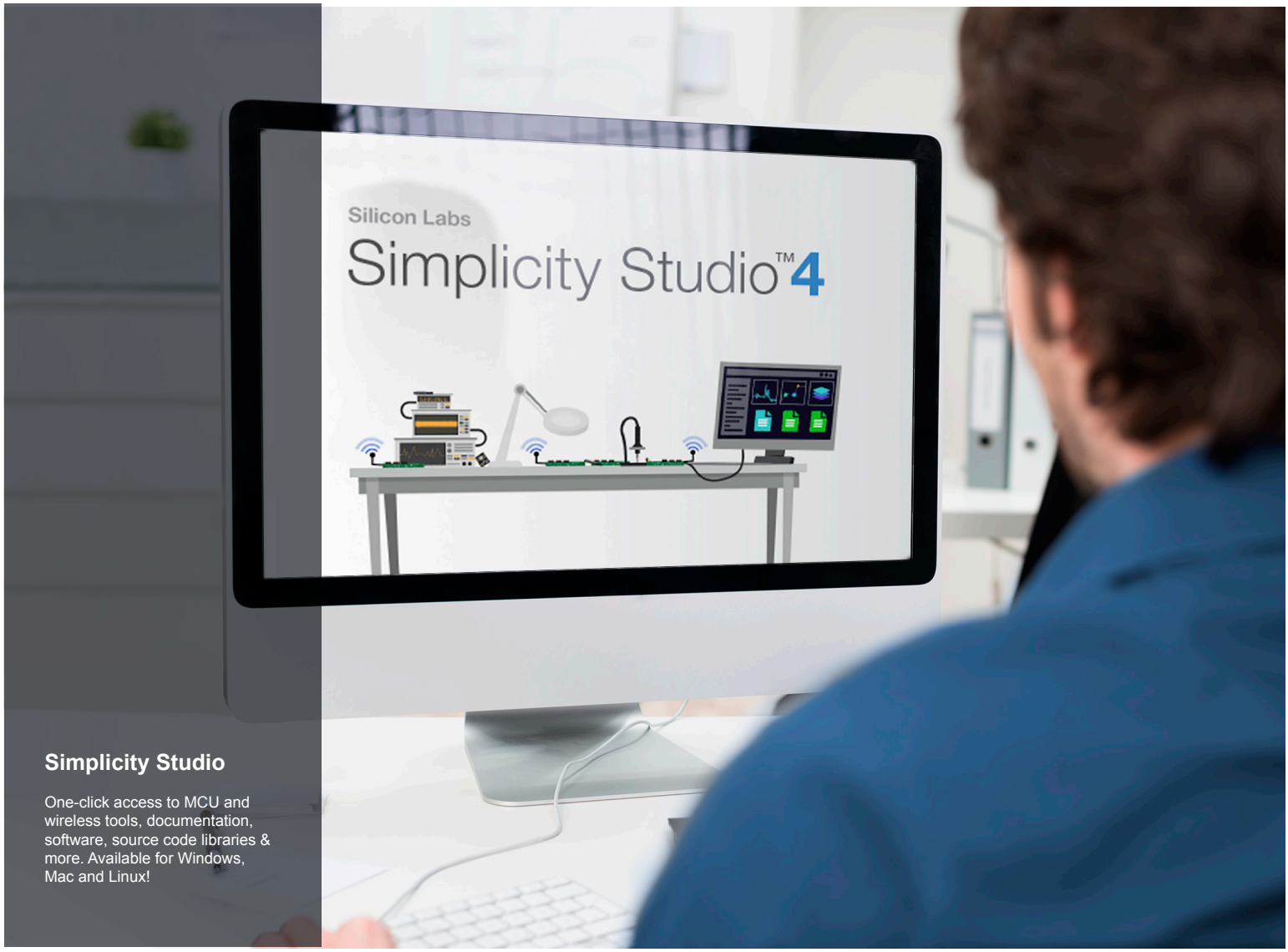
September, 2016

- Moved UID_E101 and PKG_E103 from the errata to the errata history.
- Added WDT_E101.

Revision 0.1

February, 2014

- Initial release.



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Silicon Laboratories Inc.
400 West Cesar Chavez
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