Product Change Notification - SYST-27MOSW029

Date:

30 Nov 2018

Product Category:

Ethernet Switches

Affected CPNs:

Notification subject:

Data Sheet - KSZ9477S 7-Port Gigabit Ethernet Switch with Ring Redundancy, SGMII and RGMII/MI Data Sheet Document Revision

Notification text:

SYST-27MOSW029

Microchip has released a new DeviceDoc for the KSZ9477S 7-Port Gigabit Ethernet Switch with Ring Redundancy, SGMII and RGMII/MI of devices. If you are using one of these devices please read the document located at KSZ9477S 7-Port Gigabit Ethernet Switch with Ring Redundancy, SGMII and RGMII/MI.

Notification Status: Final

Description of Change: Below are the changes

Section/Figure/Entry	Correction
Section 8.1, "Package Mark- ing Information," on page 255	Updated top marking information.
Section 8.2, "Package Draw- ings," on page 256	Updated package drawings.
Table 4-2, "Enabling and Disabling Quiet-WIRE"	Updated MMD Quiet-WIRE Configuration 3 Regis- ter “Disable Quiet-WIRE” entry.
Table 4-17, "Matching Rule Options"	Table updated.
Section 4.4.9, "Tail Tagging Mode," on page 41	Section updated. Added PTP specific content.
Section 4.1.11, "LinkMD®+ Enhanced Diagnostics: Receive Signal Quality Indi- cator," on page 26	Updated LinkMD+ text.
Section 4.1.8, "Quiet-WIRE Filtering," on page 24, Sec- tion 5.4, "MDIO Manage- able Device (MMD) Registers (Indirect)," on page 220	Updated functional description and added Quiet-Wire register descriptions.
Section 4.1.10, "LinkMD® Cable Diagnostics," on page 25	LinkMD details added.
Section 4.4.15, "Low Latency Cut-Through Mode," on page 45	Minor text clarification.
Section 4.4.2.4, "Learning," on page 32	Text correction.
Section 4.4.2.6, "Aging," on page 32	Corrected “time stamp” to “age count” in multiple locations.
Section 5.2.2.5, "PHY Auto-Negotiation Advertisement Register," on page 160	Changed default value of Pause (Flow Control) Capability bit to a note referencing the LED1_1 configuration strap.
Section 5.2.2.10, "PHY 1000BASE-T Control Regis- ter," on page 164	Corrected bit 10 default value. Added information on Test Mode Bits 15:13.

Section 5.2.8.4, "Port Authentication Control Reg- ister," on page 190	Corrected bits 1:0 description.
Section 5.1.6.11, "Global PTP Message Config 1 Reg- ister," on page 125	Corrected 802.3AS to 802.1AS and added descrip- tions.
Section 5.2.2.16, "PHY LinkMD Register," on page 168	Updated register bit descriptions.
Section 5.1.1.4, "Global Chip ID 3 Register," on page 75	Corrected bit 0 description.
Section 5.4, "MDIO Manage- able Device (MMD) Regis- ters (Indirect)," on page 220	Added definitions for MMD Signal Quality Register (ACh) and MMD Quiet-WIRE Configuration Regis- ters (25h-34h).
Section 5.4, "MDIO Manage- able Device (MMD) Regis- ters (Indirect)," on page 220	Corrected the MMD register read example.
Section 5.4.8, "MMD Quiet- WIRE Configuration 1 Reg- ister," on page 223, Section 5.4.9, "MMD Quiet-WIRE Configuration 2 Register," on page 223, Section 5.4.10, "MMD Quiet-WIRE Configu- ration 3 Register," on page 224	Updated default value fields.
Table 6-2, “RGMII Timing Values,” on page 239	Revised minimum RGMII TSKEW parameter.
Table 3-3, “Configuration Strap Descriptions,” on page 18	Corrected swapping of LED2_0 and LED4_0, added notes in strapping. Corrected RXD6_0 in strapping table.
Table 1-3, “Register Nomen- clature,” on page 7	Added additional W0C “Write zero to clear” bit type.
Section 5.5.1, "SGMII Con- trol Register," on page 228	Corrected defaults and bit types. Added details and updated bit names.
Section 5.5.2, "SGMII Status Register," on page 229	Corrected defaults and bit types. Updated Link Sta- tus description.
Section 5.5.5, "SGMII Auto- Negotiation Advertisement Register," on page 230	Added additional description.
Section 5.5.6, "SGMII Auto- Negotiation Link Partner Base Ability Register," on page 231, Section 5.5.7, "SGMII Auto- Negotiation Expansion Register," on page 232	Added new register definitions.
Section 5.5.8, "SGMII Digital Control Register," on page 232, Section 5.5.9, "SGMII Auto- Negotiation Control Register," on page 233, Section 5.5.10, "SGMII Auto- Negotiation Status Register," on page 234	Added additional description.
Section 5.1.3.1, "Power Down Control 0 Register," on page 85	Added SGMII-specific information to bits 4:3 description.
Section 5.2.1.5, "Port Inter- rupt Status Register," on page 153, Section 5.2.1.6, "Port Interrupt Mask Regis- ter," on page 154	Updated bit 3.
Section 5.1.7.14, "Global HSR AME Control Register 0," on page 148	Made bit 6 reserved.

Section 2.1, "General Description," on page 8, Section 4.14.4, "Serial Giga- bit Media Independent Inter- face (SGMII) (Port 7)," on page 70	Updated SGMII description.
Section 4.10, "Power," on page 59	Corrected reference to AVDDH.

Impacts to Data Sheet: None

Reason for Change: To Improve Manufacturability

Change Implementation Status: Complete

Date Document Changes Effective: 30 Nov 2018

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):

KSZ9477S 7-Port Gigabit Ethernet Switch with Ring Redundancy, SGMII and RGMII/MI

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Affected Catalog Part Numbers (CPN)

KSZ9477STXI
KSZ9477STXI-TR