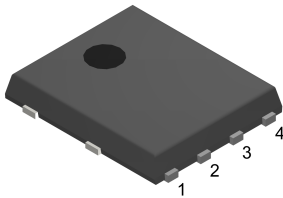
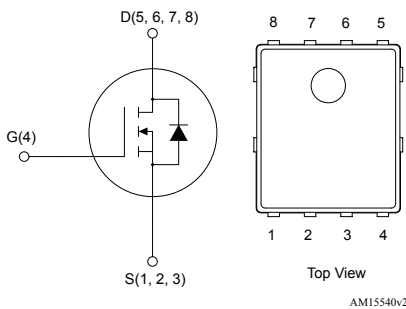


## N-channel 100 V, 20 mΩ typ., 10 A STripFET F7 Power MOSFET in a PowerFLAT 5x6 package


**PowerFLAT 5x6**


### Features

Order code	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$	$P_{TOT}$
STL40N10F7	100 V	24 mΩ	10 A	5 W

- Among the lowest  $R_{DS(on)}$  on the market
- Excellent FoM (figure of merit)
- Low  $C_{rSS}/C_{iSS}$  ratio for EMI immunity
- High avalanche ruggedness

### Applications

- Switching applications

### Description

This N-channel Power MOSFET utilizes STripFET F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.



#### Product status link

[STL40N10F7](#)

#### Product summary

<b>Order code</b>	STL40N10F7
<b>Marking</b>	40N10F7
<b>Package</b>	PowerFLAT 5x6
<b>Packing</b>	Tape and reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	100	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	40	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	28	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	10	A
	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	7	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	40	A
$P_{TOT}^{(1)}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	70	W
$P_{TOT}^{(2)}$	Total power dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	5	W
$T_{stg}$	Storage temperature range	- 55 to 175	$^\circ\text{C}$
$T_J$	Operating junction temperature range		$^\circ\text{C}$

1. This value is rated according to  $R_{thj-c}$ .
2. This value is rated according to  $R_{thj-pcb}$ .
3. Pulse width is limited by safe operating area.

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max.	2.08	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max.	30	

1. When mounted on a 1-inch<sup>2</sup> FR-4 board, 2oz Cu,  $t < 10\text{ s}$ .

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 3. On/Off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	100			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 100\text{ V}$			10	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 100\text{ V}$ , $T_C = 125\text{ °C}$			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 10\text{ A}$		20	24	m $\Omega$

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 50\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	1270	-	pF
$C_{oss}$	Output capacitance		-	290	-	pF
$C_{rSS}$	Reverse transfer capacitance		-	24	-	pF
$Q_g$	Total gate charge	$V_{DD} = 50\text{ V}$ , $I_D = 32\text{ A}$ , $V_{GS} = 10\text{ V}$ (see Figure 13. Test circuit for gate charge behavior)	-	19	-	nC
$Q_{gs}$	Gate-source charge		-	9	-	nC
$Q_{gd}$	Gate-drain charge		-	4.5	-	nC

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 50\text{ V}$ , $I_D = 16\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	12	-	ns
$t_r$	Rise time		-	17.5	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 12. Test circuit for resistive load switching times)	-	22	-	ns
$t_f$	Fall time		-	5.6	-	ns

**Table 6. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current	$I_{SD} = 32\text{ A}$ , $V_{GS} = 0\text{ V}$	-		32	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				128	A
$V_{SD}^{(2)}$	Forward on voltage				1.1	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 32\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,	-	41		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 80\text{ V}$ , $T_J = 150^\circ\text{ C}$	-	47		nC
$I_{RRM}$	Reverse recovery current	(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	2.3		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

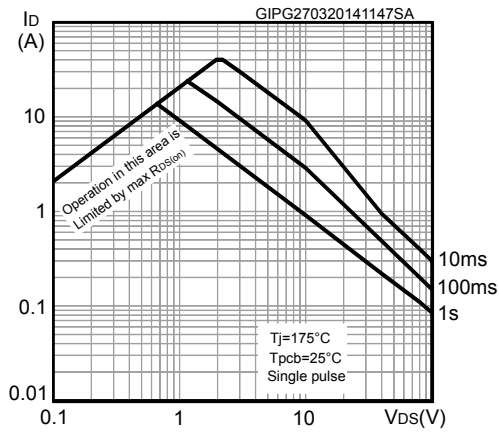


Figure 2. Thermal impedance

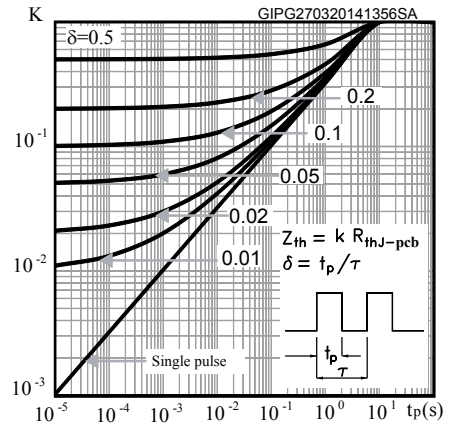


Figure 3. Output characteristics

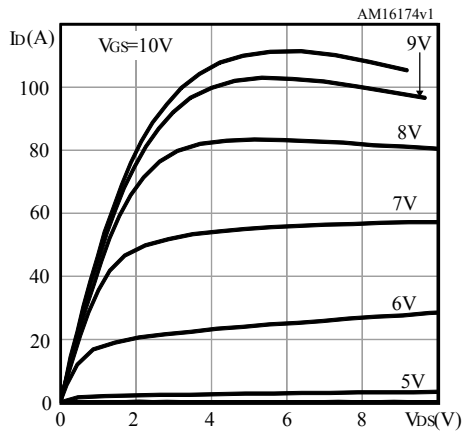


Figure 4. Transfer characteristics

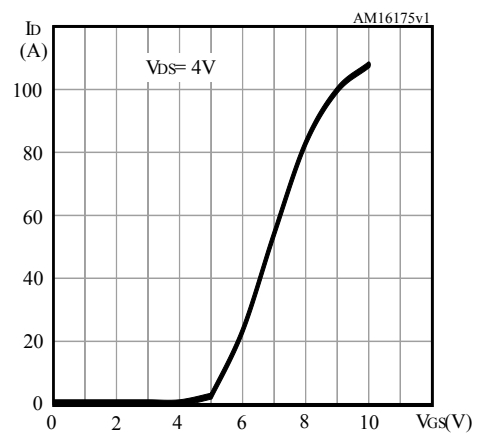


Figure 5. Gate charge vs gate-source voltage

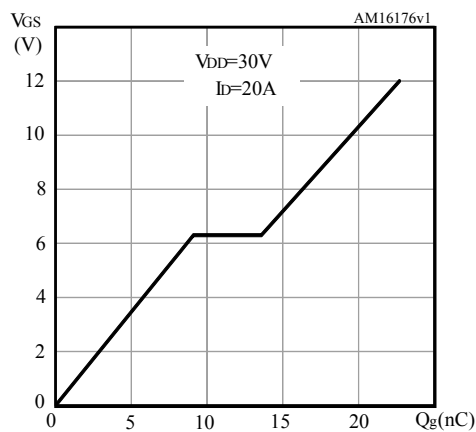


Figure 6. Static drain-source on-resistance

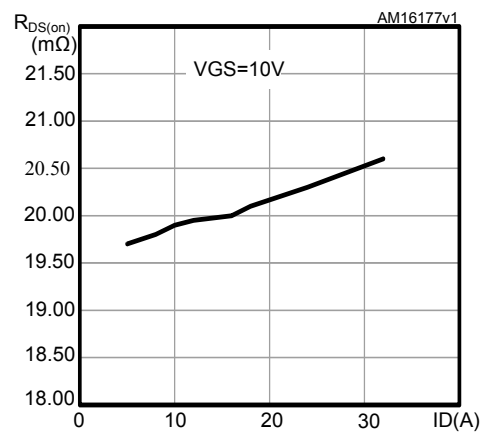


Figure 7. Capacitance variations

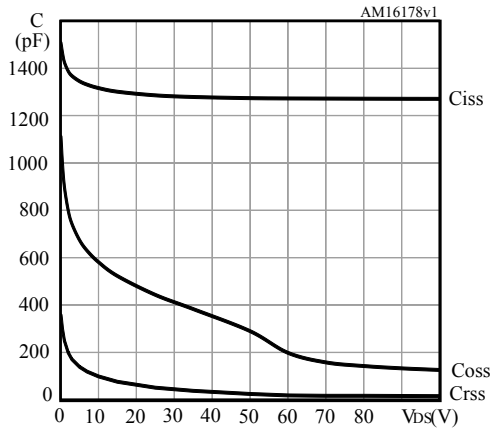


Figure 8. Normalized gate threshold voltage vs temperature

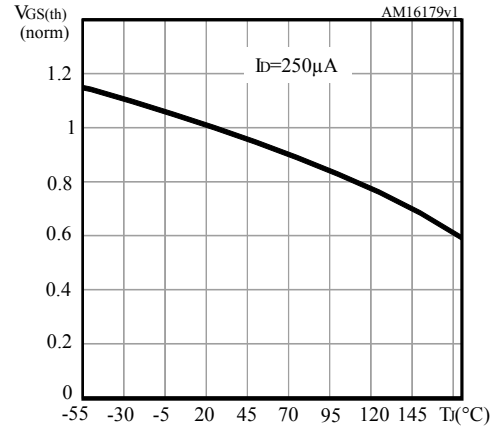


Figure 9. Normalized on-resistance vs temperature

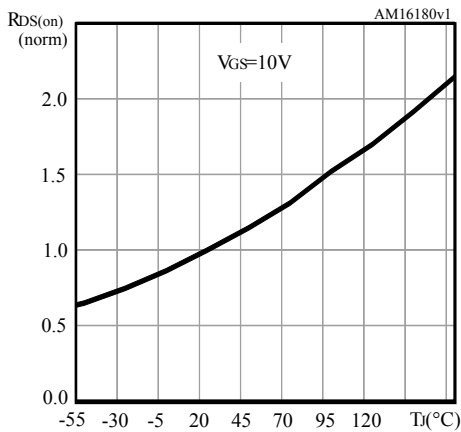


Figure 10. Normalized V<sub>(BR)DSS</sub> vs temperature

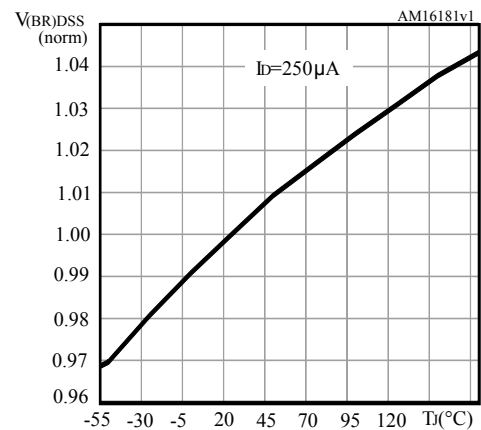
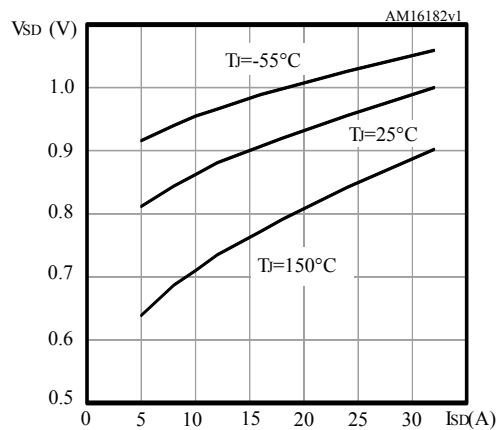


Figure 11. Source-drain diode forward characteristics



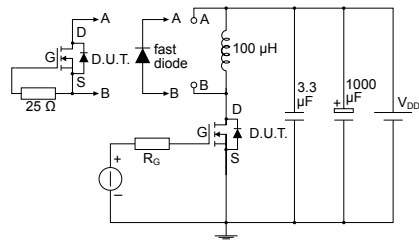
### 3 Test circuits

**Figure 12. Test circuit for resistive load switching times**


AM01468v1

**Figure 13. Test circuit for gate charge behavior**


AM01469v1

**Figure 14. Test circuit for inductive load switching and diode recovery times**


AM01470v1

**Figure 15. Unclamped inductive load test circuit**


AM01471v1

**Figure 16. Unclamped inductive waveform**


AM01472v1

**Figure 17. Switching time waveform**

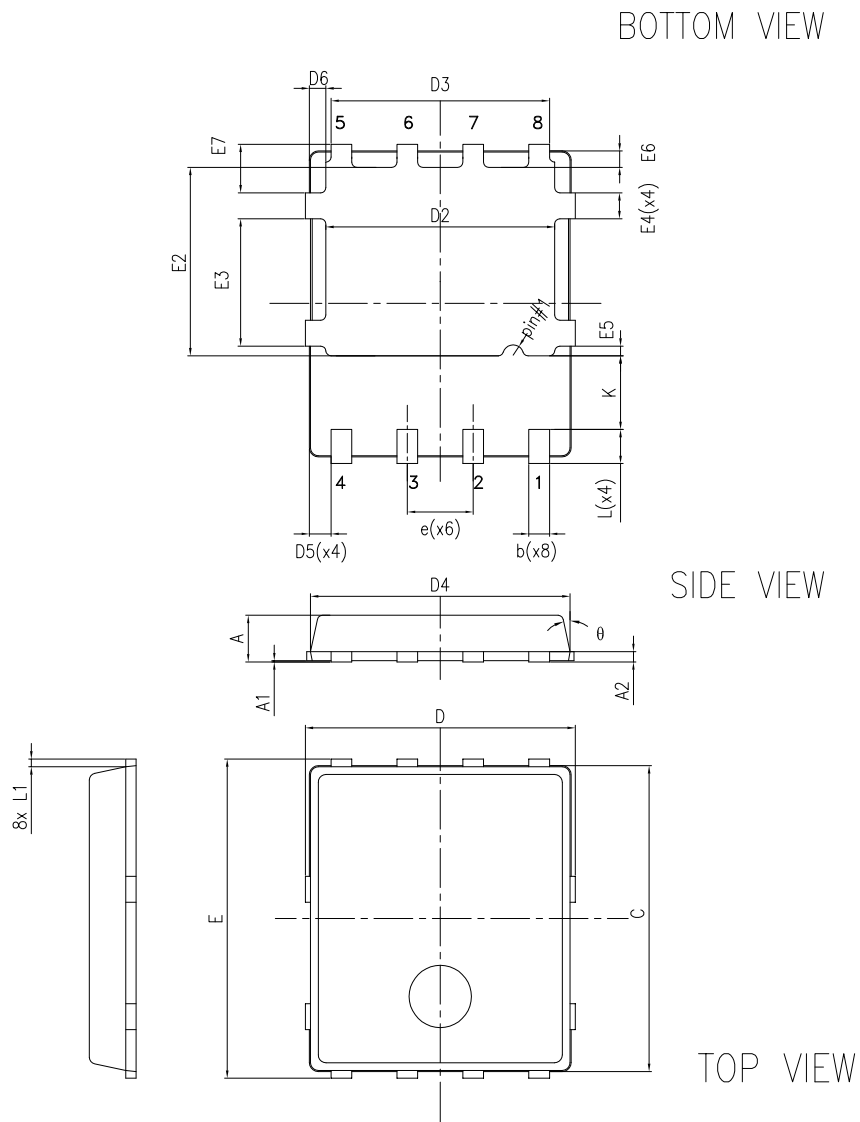

AM01473v1

## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 PowerFLAT 5x6 type R package information

**Figure 18. PowerFLAT 5x6 type R package outline**



A0ER\_8231817\_Rev20

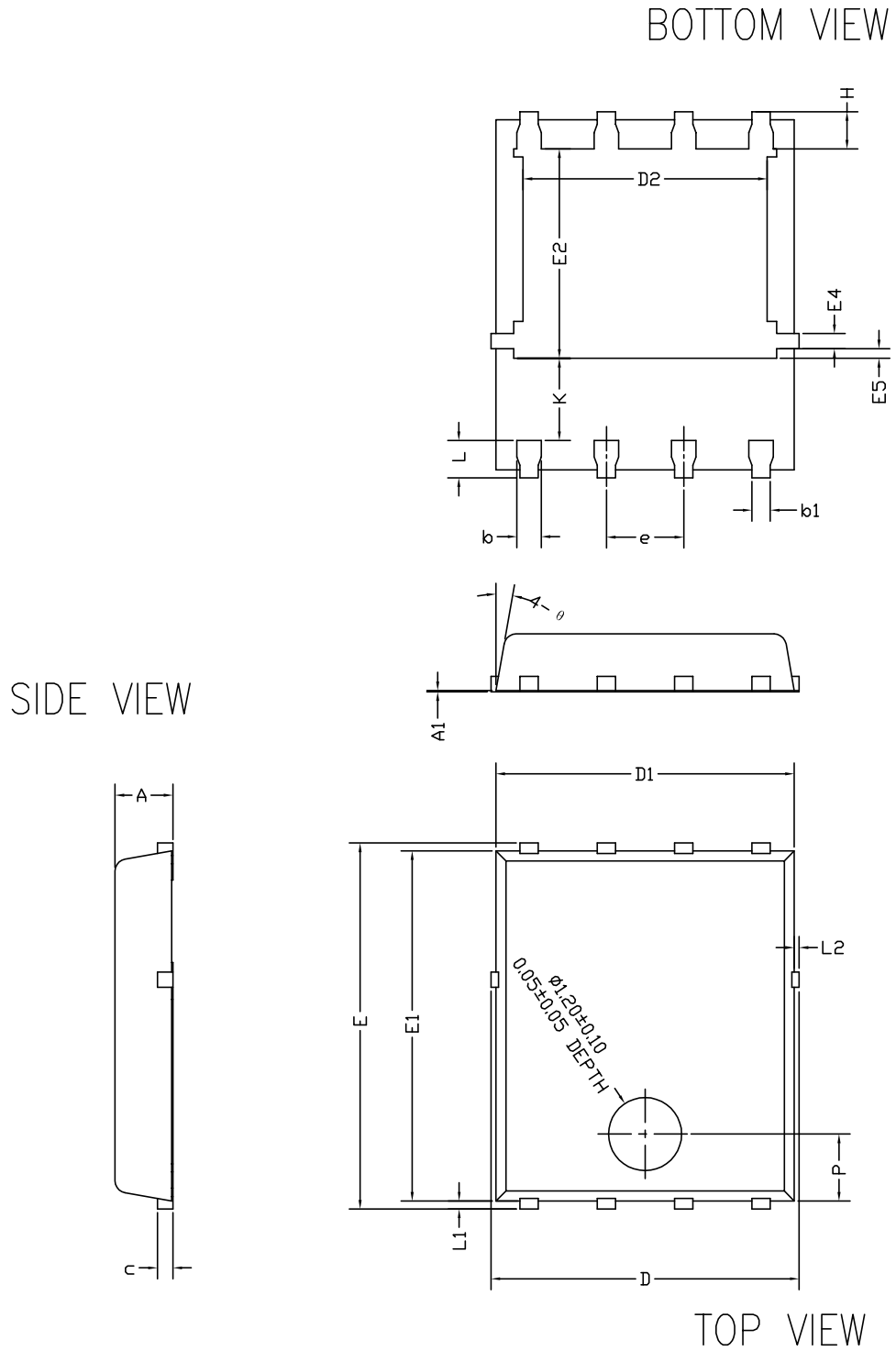


**Table 7. PowerFLAT 5x6 type R mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.20
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	5.95	6.15	6.35
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.75	0.90	1.05
K	1.275		1.575
L	0.60		0.80
L1	0.05	0.15	0.25
θ	0°		12°

## 4.2 PowerFLAT 5x6 type R SUBCON package information

Figure 19. PowerFLAT 5x6 type R SUBCON package outline

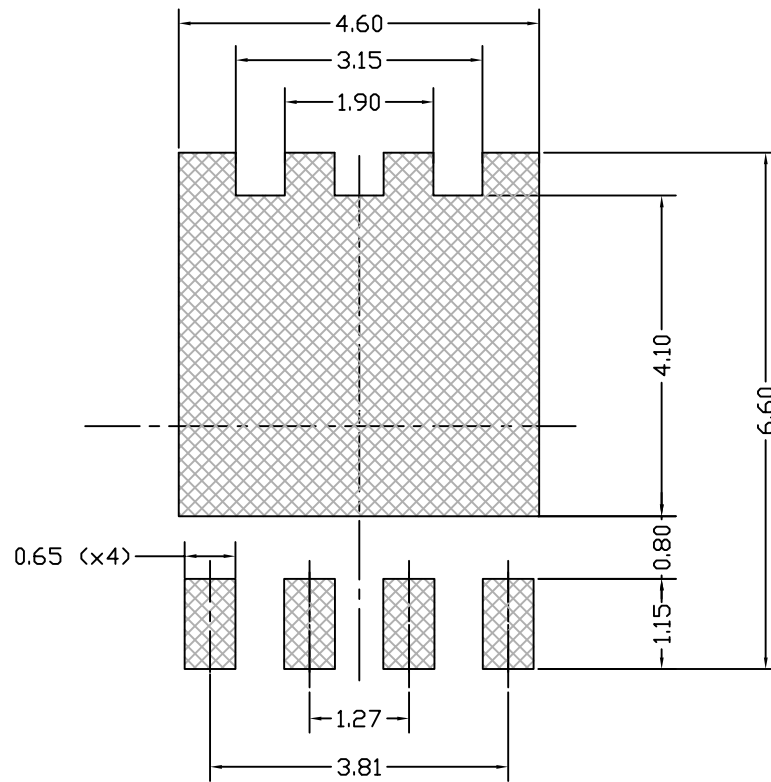


8472137\_SUBCON\_998G\_Type\_R\_REV4

**Table 8. PowerFLAT 5x6 type R SUBCON package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.90	0.95	1.00
A1		0.02	
b	0.35	0.40	0.45
b1		0.30	
c	0.21	0.25	0.34
D			5.10
D1	4.80	4.90	5.00
D2	3.91	4.01	4.11
e	1.17	1.27	1.37
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.34	3.44	3.54
E4	0.15	0.25	0.35
E5	0.06	0.16	0.26
H	0.51	0.61	0.71
K	1.10		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
L2			0.10
P	1.00	1.10	1.20
θ	8°	10°	12°

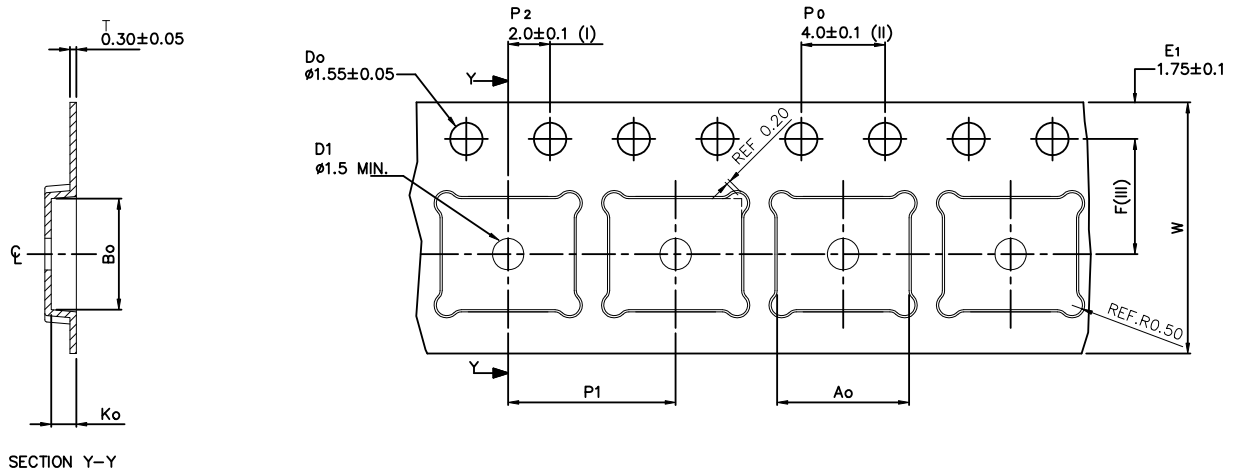
Figure 20. PowerFLAT 5x6 recommended footprint (dimensions are in mm)



8231817\_FOOTPRINT\_simp\_Rev\_20

### 4.3 PowerFLAT 5x6 packing information

Figure 21. PowerFLAT 5x6 tape (dimensions are in mm)



A <sub>0</sub>	6.30	+/- 0.1
B <sub>0</sub>	5.30	+/- 0.1
K <sub>0</sub>	1.20	+/- 0.1
F	5.50	+/- 0.1
P <sub>1</sub>	8.00	+/- 0.1
W	12.00	+/- 0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.

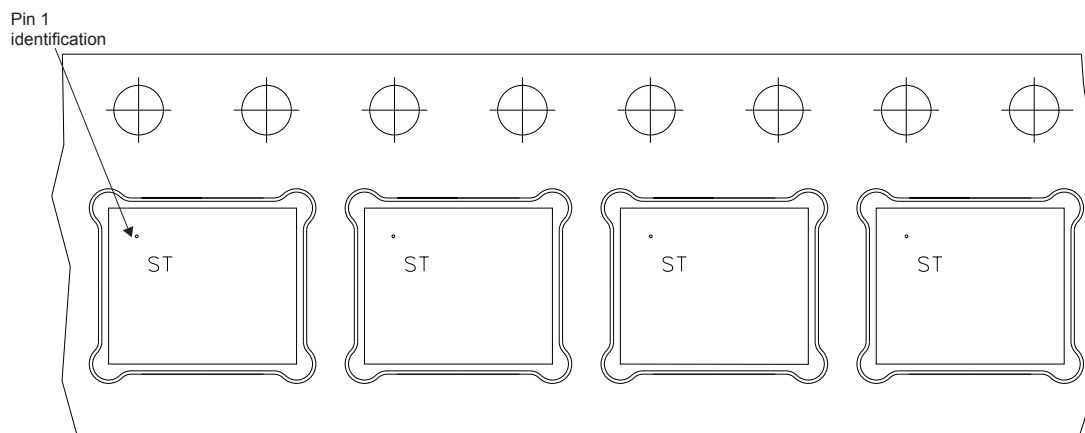
(II) Cumulative tolerance of 10 sprocket holes is  $\pm 0.20$ .

(III) Measured from centreline of sprocket hole to centreline of pocket

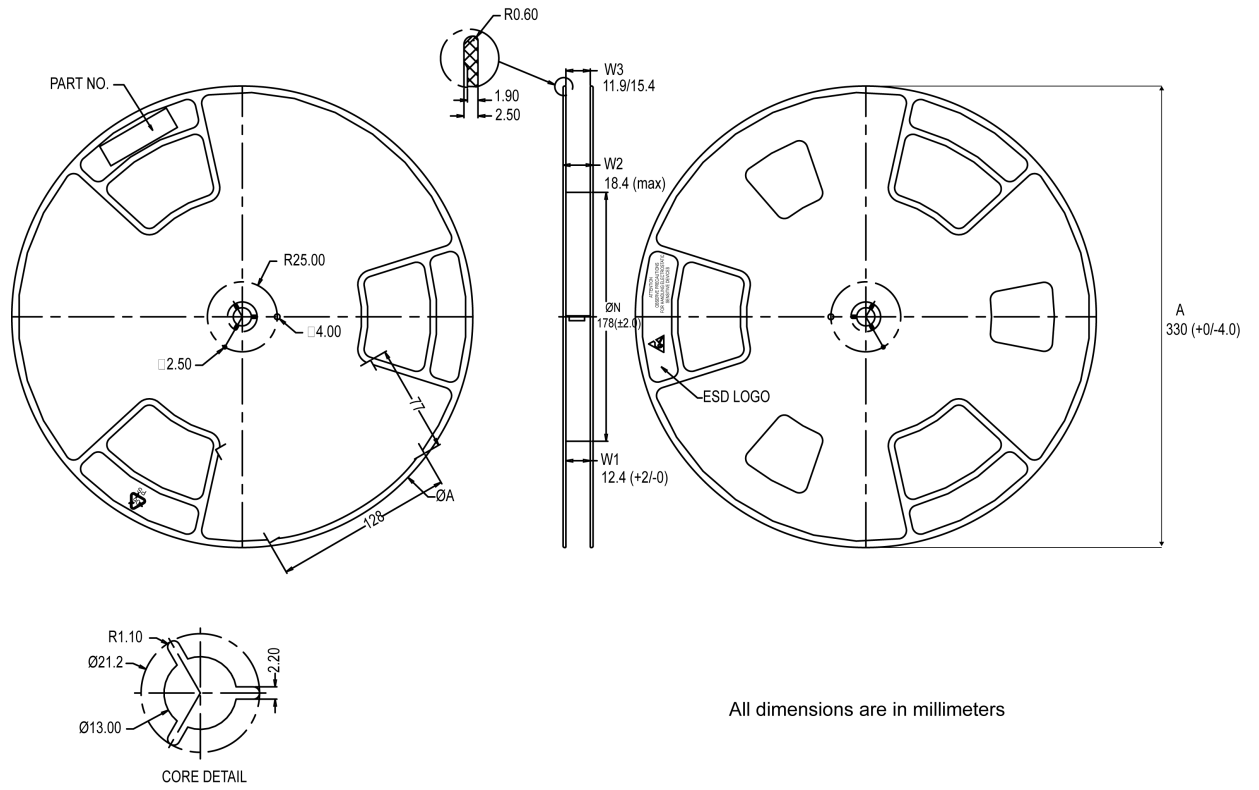
Base and bulk quantity 3000 pcs  
All dimensions are in millimeters

8234350\_Tape\_rev\_C

Figure 22. PowerFLAT 5x6 package orientation in carrier tape



**Figure 23. PowerFLAT 5x6 reel**



All dimensions are in millimeters

8234350\_Reel\_rev\_C

## Revision history

**Table 9. Document revision history**

Date	Revision	Changes
20-May-2015	1	First release.
02-Nov-2015	2	Document status promoted from preliminary to production data. Modified: $V_{GS(th)}$ values in tab 4. Updated the entire typical values in tab 5, tab 6 and tab7 Added Electrical characteristics (curves) Updated Figure 13, 14, 15 and 16 Minor text changes.
18-Dec-2015	3	Updated title, features and description. Updated <i>Table 2: "Absolute maximum ratings"</i> and <i>Table 4: "On/Off states"</i> . Minor text changes.
01-Feb 2016	4	Updated <i>Table 5: "Dynamic"</i> . Minor text changes.
21-Feb-2020	5	Updated <a href="#">Section 4 Package information</a> . Minor text changes.

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