Revision History

PCN#	Issue Date	Description
01A-22	April 4, 2022	Initial release

Subject: PCN#01A-22 Notification of Changes to CrossLink-NX™ Data Sheet and Certus-NX™ Data Sheet

Dear Lattice Customer,

Lattice Semiconductor is providing this notification of changes to the CrossLink-NX Family Data Sheet (FPGA-DS-02049) and Certus-NX Family Data Sheet (FPGA-DS-02078)

Change Description

There are 3 distinct changes being made to the datasheets. Each of them is described below. These changes will be included in the new CrossLink-NX Family Data Sheet (FPGA-DS-02049 version 1.3 dated April 2022) and Certus-NX Family Data Sheet (FPGA-DS-02078 version 1.1 dated April 2022)

Functionality support on certain speed grades
The -7 speed grade of the commercial and industrial devices are being updated to remove the support for functionality in the following four blocks.

- Analog to Digital Converter (ADC)
- Input Comparator
- Digital Temperature Readout (DTR)
- Error Correction Coding (ECC) function within the Embedded Block Ram (EBR)

Specific datasheet sections have been updated to reflect this change. The datasheet sections to reference are: 1.1, 2.5.1, 3.21, 3.23, 6.1

Device Performance Values in specific tables
Several values are being updated in the Device Performance sections of the datasheet. This is being done to reflect final characterization values as part of the completion of family characterization. The specific tables affected by the changes are listed below

When reviewing their design implementations, customers should pay particular attention to the following specific specifications or sections as these parameters have been adversely changed and may impact design performance.

- LVCMOS12 and LVCMOS10 values in Tables 3.14 and 4.14
- D-PHY Output Impedance and Low Power Mode VOH in Tables 3.24 and 4.24
- Generic DDRX1 performance in Tables 3.31 and 4.31
- All updated parameters in Tables 3.35 and 4.35
- User I/O enabled wakeup timing in Tables 3.46 and 4.45

The complete list of affected tables are as follows:

Commercial/Industrial Tables:

- 3.13 - sysI/O Recommended Operating Conditions

- 3.14 - sysI/O Single-Ended DC Electrical Characteristics
- 3.15 - sysI/O DC Electrical Characteristics – High Performance I/O
- 3.24 - Soft D-PHY Output Timing and Levels
- 3.27 - Maximum I/O Buffer Speed
- 3.31 – External Switching Characteristics
- 3.35 - ADC Specifications
- 3.38 – PCIe (2.5Gbps)
- 3.41 - sysCONFIG Port Timing Specifications (Certus-NX Datasheet)
- 3.46 - sysCONFIG Port Timing Specifications (Crosslink-NX Datasheet)

Automotive Performance Tables:

- 4.14 - sysI/O Single-Ended DC Electrical Characteristics
- 4.15 - sysI/O DC Electrical Characteristics – High Performance I/O
- 4.24 - Soft D-PHY Output Timing and Levels
- 4.31 – External Switching Characteristics
- 4.35 - ADC Specifications
- 4.37 - sysCONFIG Port Timing Specifications (Certus-NX Datasheet)
- 4.38 - Hardened D-PHY Input Timing and Levels (Croslink-NX Datasheet only)
- 4.45 - sysCONFIG Port Timing Specifications (Crosslink-NX Datasheet)

Please note that the silicon has not been updated and the silicon performance has not changed from any previous material shipments. We are only updating the datasheet performance numbers to match the silicon characteristics.

HPIO LVDS/sub-LVDS inputs
The supply operating range for HPIO LVDS/sub-LVDS inputs is being expanded to support additional Vccio ranges. The current specification only supports 1.8V Vccio. The updated specification expands support to 1.2V, 1.35V, 1.5V, and 1.8V. This update is located in *Table 3.13. sysI/O Recommended Operating Conditions (Commercial/Industrial) and Table 4.13. sysI/O Recommended Operating Conditions (Automotive).*

Please be aware – With the additional support of the lower supply voltages, customer design must also limit the input voltage levels accordingly. Please refer to the updated footnotes in Table 3.13 and 4.13

Affected Products

All Ordering part numbers for the Crosslink-NX and Certus-NX device families are affected by this PCN.

Note: This PCN also affects all package, grade and tape/reel options and any custom devices (i.e. factory programmed, special test, etc.) which are derived from any of the base devices listed in the family.

Datasheet Specifications

The updated CrossLink-NX Family Data Sheet (FPGA-DS-02049 version 1.3 dated April 2022) and Certus-NX Family Data Sheet (FPGA-DS-02078 version 1.1 dated April 2022) with the above changes will be available from the Lattice website on 4/8/22.

Recommended Action

The following customer actions are recommended for each of the datasheet changes being implemented.

Functionality support on certain speed grades
All customers using the -7 Commercial/Industrial speed grade should review their current or in progress designs to determine if they utilize any of the affected blocks which are being addressed in this PCN. If the customer is using these features on a -7 speed grade device, they will be required to convert the ordering part number to order the equivalent -8 speed grade device. Customer should contact Lattice Technical Support for assistance in making this ordering part conversion.

Device Performance Values in specific tables
All customers should review the details of the changes for Device Performance in the datasheet and determine the impact on their design. This can be done by reviewing the tables listed on page 1 of this PCN.

LVDS/sub-LVDS inputs
Customers can immediately begin utilizing the additional Vccio ranges. Customers are advised to review all footnotes related to LVDS/sub-LVDS input usage to confirm voltage level compliance at the lower supply levels. Software support is included in the current release version R3.1.

PCN Timing

The datasheet changes are effective immediately and retroactively.

The change in support for ADC, ECC, DTR, and Input Comparator will be effective for all material shipments on or after July 1, 2022. All -7 speed grade material shipped prior to July 1, 2022 will still provide support for ADC and ECC functionality. Individual units can also be verified based on the top side Marking Date Code.

- Functionality still supported on -7 speed grade – Date Code is WW26'22 or earlier
- Functionality not supported on -7 speed grade – Date Code is WW27'22 or later

Additional design rule checks will be added to Radiant to notify customers of the usage of ADC, ECC, DTR, and Input Comparator blocks. The June'22 release of Radiant Version 3.2 will include these additional design rule checks.

Lattice PCNs are available on the Lattice website. Please sign up to receive e-mail PCN alerts by registering here. If you already have a Lattice web account and wish to receive PCN alerts, you can do so by logging into your account and making edits to your subscription options.

Sincerely,

Lattice PCN Administration