

# 8K x 8 Static RAM

## Features

- 55, 70 ns access times
- CMOS for optimum speed/power
- Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{OE}$  features
- TTL-compatible inputs and outputs
- Automatic power-down when deselected

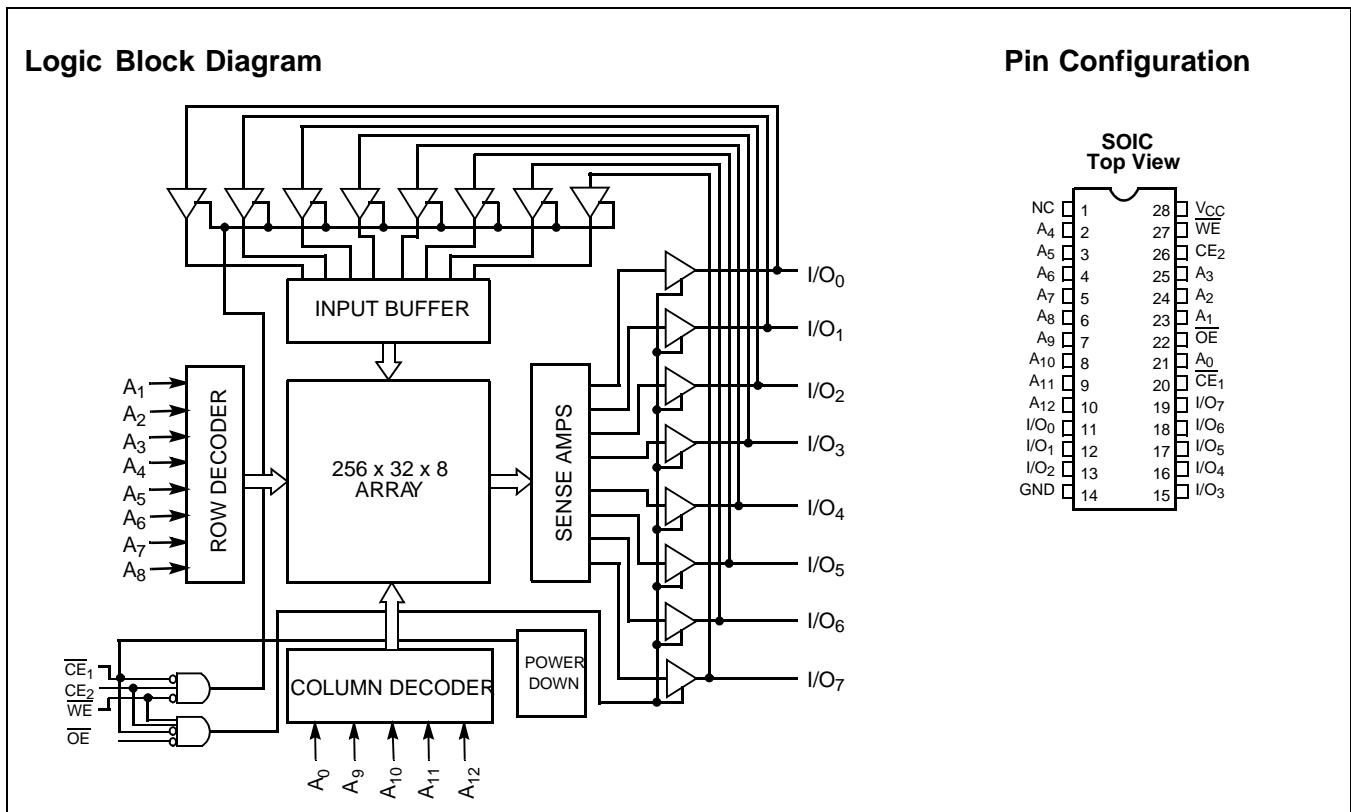
## Functional Description

The CY6264 is a high-performance CMOS static RAM organized as 8192 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE}_1$ ), an active HIGH chip enable ( $CE_2$ ), and active LOW output enable ( $\overline{OE}$ ) and three-state drivers. Both devices have an automatic

power-down feature ( $\overline{CE}_1$ ), reducing the power consumption by over 70% when deselected. The CY6264 is packaged in a 450-mil (300-mil body) SOIC.

An active LOW write enable signal ( $\overline{WE}$ ) controls the writing/reading operation of the memory. When  $\overline{CE}_1$  and  $\overline{WE}$  inputs are both LOW and  $CE_2$  is HIGH, data on the eight data input/output pins ( $I/O_0$  through  $I/O_7$ ) is written into the memory location addressed by the address present on the address pins ( $A_0$  through  $A_{12}$ ). Reading the device is accomplished by selecting the device and enabling the outputs,  $\overline{CE}_1$  and  $\overline{OE}$  active LOW,  $CE_2$  active HIGH, while  $\overline{WE}$  remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ( $\overline{WE}$ ) is HIGH. A die coat is used to insure alpha immunity.



**Selection Guide**

		<b>CY6264-55</b>	<b>CY6264-70</b>	<b>Unit</b>
Maximum Access Time		55	70	ns
Maximum Operating Current	Commercial	100	100	mA
	Industrial		200	
Maximum Standby Current	Commercial	20/15	20/15	mA
	Industrial		30	

Shaded areas contain advance information.

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with  
 Power Applied..... -55°C to +125°C  
 Supply Voltage to Ground Potential ..... -0.5V to +7.0V  
 DC Voltage Applied to Outputs  
 in High Z State<sup>[1]</sup> ..... -0.5V to +7.0V  
 DC Input Voltage<sup>[1]</sup>..... -0.5V to +7.0V

Output Current into Outputs (LOW)..... 20 mA  
 Static Discharge Voltage..... >2001V  
 (per MIL-STD-883, Method 3015)  
 Latch-Up Current..... >200 mA

**Operating Range**

<b>Range</b>	<b>Ambient Temperature</b>	<b>V<sub>CC</sub></b>
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	

**Electrical Characteristics** Over the Operating Range

<b>Parameter</b>	<b>Description</b>	<b>Test Conditions</b>	<b>6264-55</b>		<b>6264-70</b>		<b>Unit</b>
			<b>Min.</b>	<b>Max.</b>	<b>Min.</b>	<b>Max.</b>	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub>	2.2	V <sub>CC</sub>	V
V <sub>IL</sub>	Input LOW Voltage <sup>[1]</sup>		-0.5	0.8	-0.5	0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-5	+5	-5	+5	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[2]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		-300		-300	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA	Com'l	100	100		mA
			Ind'l			200	
I <sub>SB1</sub>	Automatic $\overline{CE}_1$ Power-Down Current	Max. V <sub>CC</sub> , $\overline{CE}_1 \geq V_{IH}$ , Min. Duty Cycle=100%	Com'l	20	20		mA
			Ind'l			40	
I <sub>SB2</sub>	Automatic $\overline{CE}_1$ Power-Down Current	Max. V <sub>CC</sub> , $\overline{CE}_1 \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V	Com'l	15	15		mA
			Ind'l			30	

Shaded areas contain advance information.

**Notes:**

1. Minimum voltage is equal to -3.0V for pulse durations less than 30 ns.
2. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

**Switching Characteristics** Over the Operating Range<sup>[3]</sup>

Parameter	Description	6264-55		6264-70		Unit
		Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>						
$t_{RC}$	Read Cycle Time	55		70		ns
$t_{AA}$	Address to Data Valid		55		70	ns
$t_{OHA}$	Data Hold from Address Change	5		5		ns
$t_{ACE1}$	$\overline{CE}_1$ LOW to Data Valid		55		70	ns
$t_{ACE2}$	$CE_2$ HIGH to Data Valid		40		70	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		25		35	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z	3		5		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[4]</sup>		20		30	ns
$t_{LZCE1}$	$\overline{CE}_1$ LOW to Low Z <sup>[5]</sup>	5		5		ns
$t_{LZCE2}$	$CE_2$ HIGH to Low Z	3		5		ns
$t_{HZCE}$	$\overline{CE}_1$ HIGH to High Z <sup>[4, 5]</sup> $CE_2$ LOW to High Z		20		30	ns
$t_{PU}$	$\overline{CE}_1$ LOW to Power-Up	0		0		ns
$t_{PD}$	$\overline{CE}_1$ HIGH to Power-Down		25		30	ns
<b>WRITE CYCLE<sup>[6]</sup></b>						
$t_{WC}$	Write Cycle Time	50		70		ns
$t_{SCE1}$	$\overline{CE}_1$ LOW to Write End	40		60		ns
$t_{SCE2}$	$CE_2$ HIGH to Write End	30		50		ns
$t_{AW}$	Address Set-Up to Write End	40		55		ns
$t_{HA}$	Address Hold from Write End	0		0		ns
$t_{SA}$	Address Set-Up to Write Start	0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	25		40		ns
$t_{SD}$	Data Set-Up to Write End	25		35		ns
$t_{HD}$	Data Hold from Write End	0		0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[4]</sup>		20		30	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z	5		5		ns

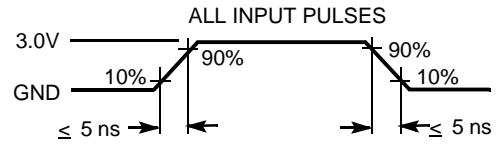
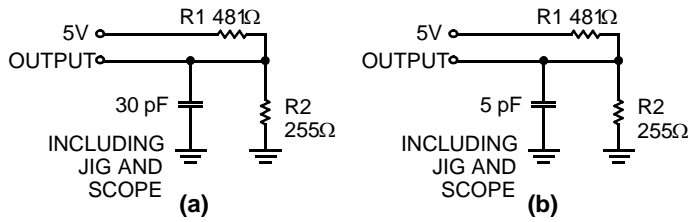
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**Capacitance<sup>[7]</sup>**

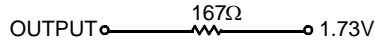
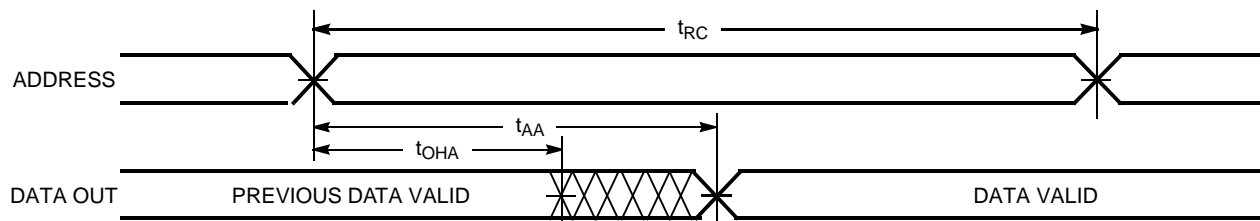
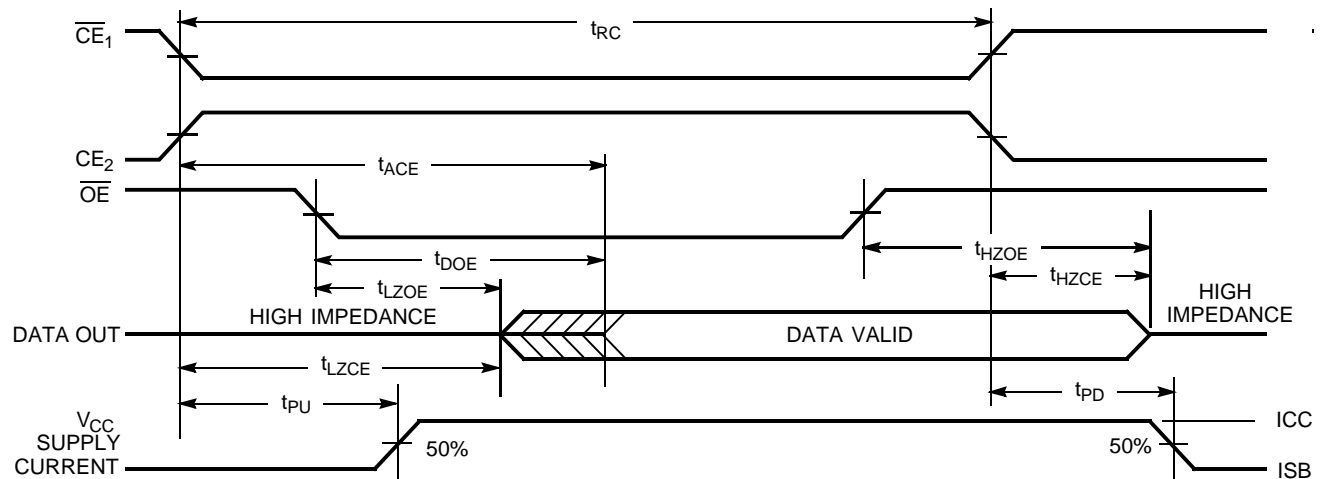
Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = 5.0\text{V}$	7	pF
$C_{OUT}$	Output Capacitance		7	pF

**Notes:**

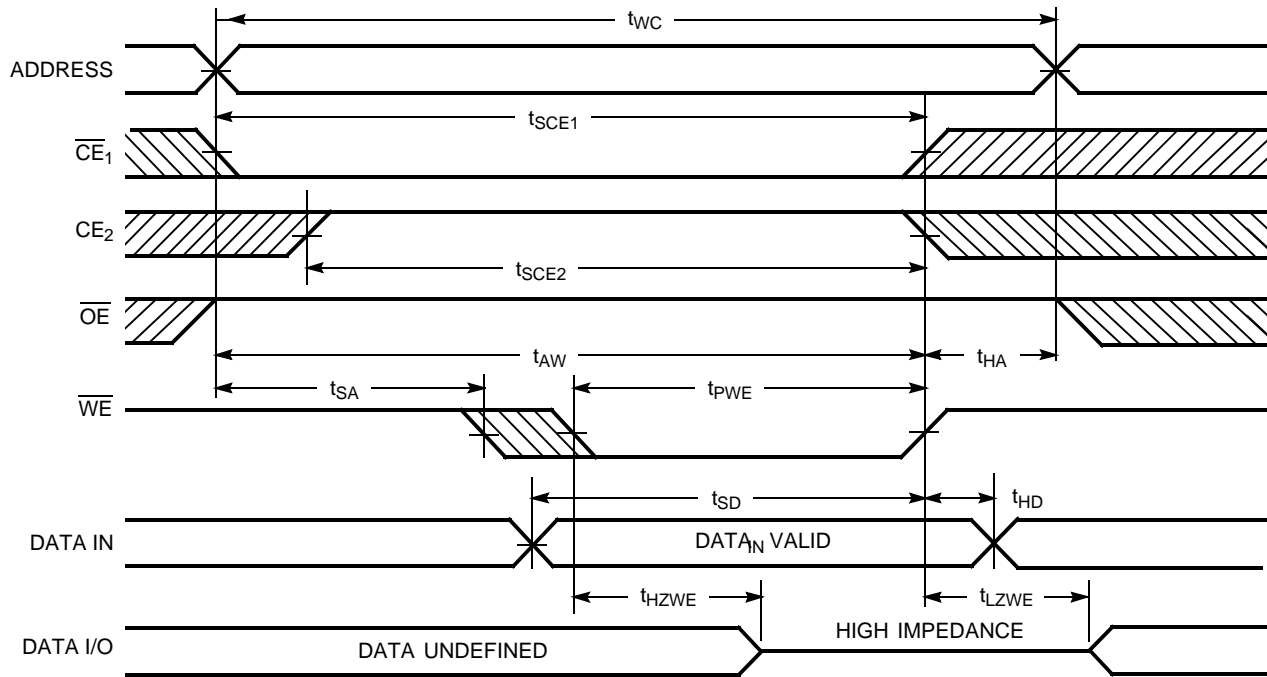
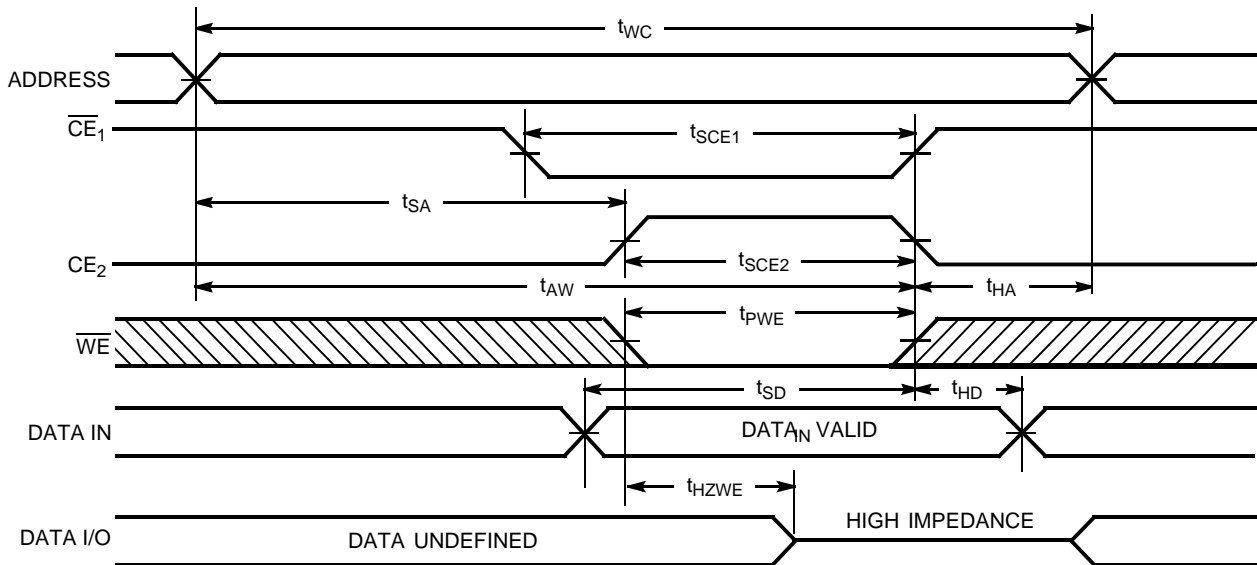
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with  $C_L = 5\text{ pF}$  as in part (b) of AC Test Loads. Transition is measured  $\pm 500\text{ mV}$  from steady-state voltage.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$  for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}_1$  LOW,  $CE_2$  HIGH, and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms**


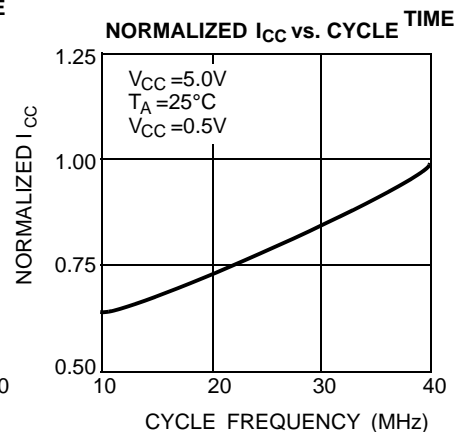
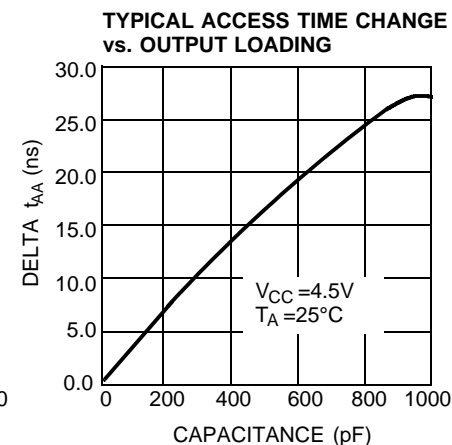
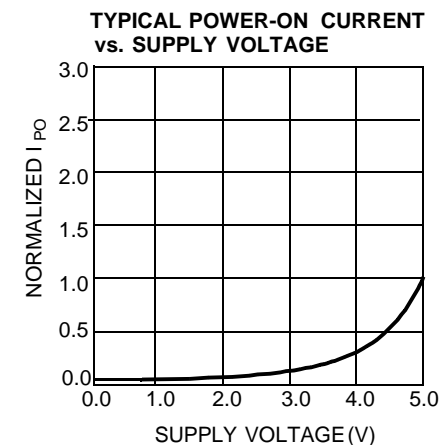
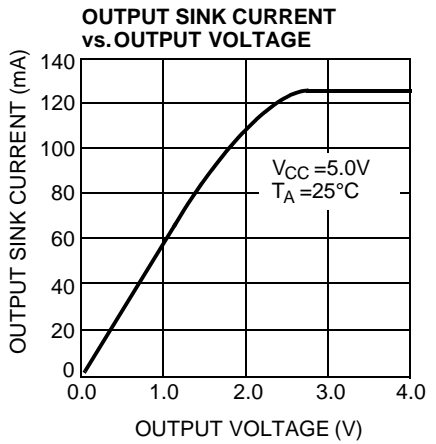
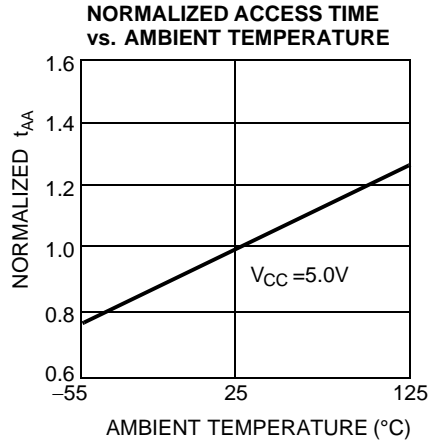
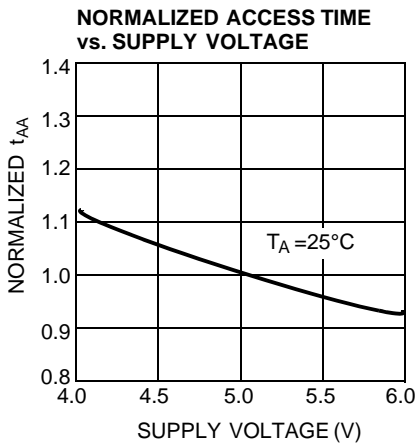
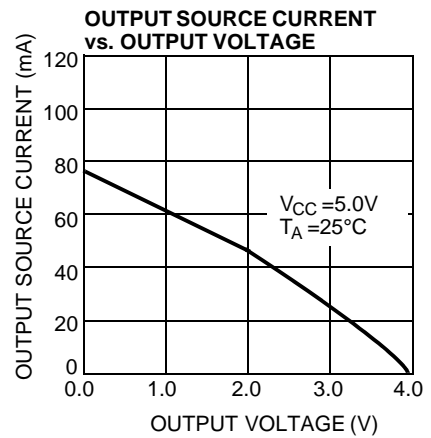
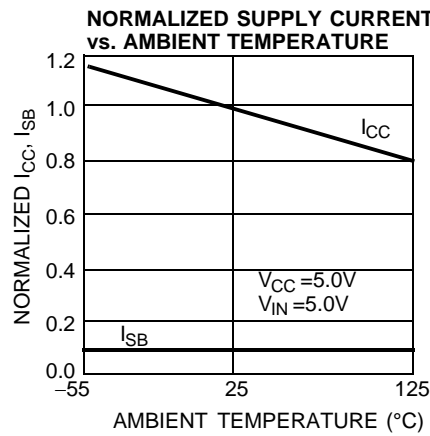
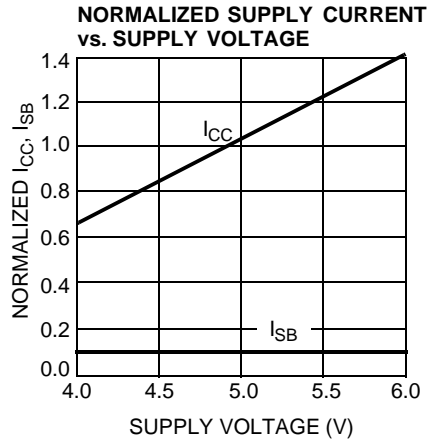
Equivalent to: THÉVENIN EQUIVALENT


**Switching Waveforms**
**Read Cycle No. 1<sup>[8, 9]</sup>**

**Read Cycle No. 2<sup>[10, 11]</sup>**

**Notes:**

8. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ .  $CE_2 = V_{IH}$ .
9. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
10.  $\overline{WE}$  is HIGH for read cycle.
11. Data I/O is High Z if  $\overline{OE} = V_{IH}$ ,  $\overline{CE}_1 = V_{IH}$ , or  $\overline{WE} = V_{IL}$ .

**Switching Waveforms (continued)**  
**Write Cycle No. 1 (WE Controlled)<sup>[9, 11]</sup>**

**Write Cycle No. 2 ( $\overline{CE}$  Controlled)<sup>[9, 11, 12]</sup>**


**Note:**  
 12. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.

**Typical DC and AC Characteristics**


**Truth Table**

$\overline{CE}_1$	$CE_2$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode
H	X	X	X	High Z	Deselect/Power-Down
X	L	X	X	High Z	Deselect
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	High Z	Deselect

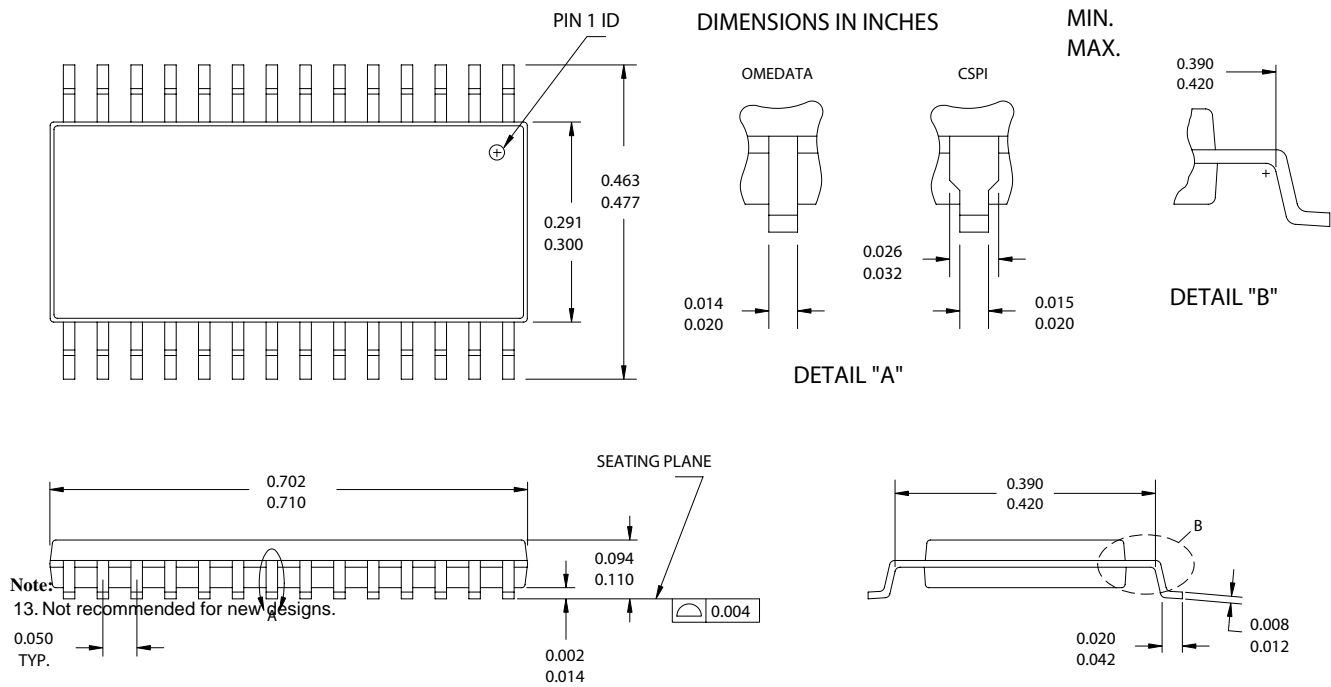
**Address Designators**

Address Name	Address Function	Pin Number
A4	X3	2
A5	X4	3
A6	X5	4
A7	X6	5
A8	X7	6
A9	Y1	7
A10	Y4	8
A11	Y3	9
A12	Y0	10
A0	Y2	21
A1	X0	23
A2	X1	24
A3	X2	25

**Ordering Information**

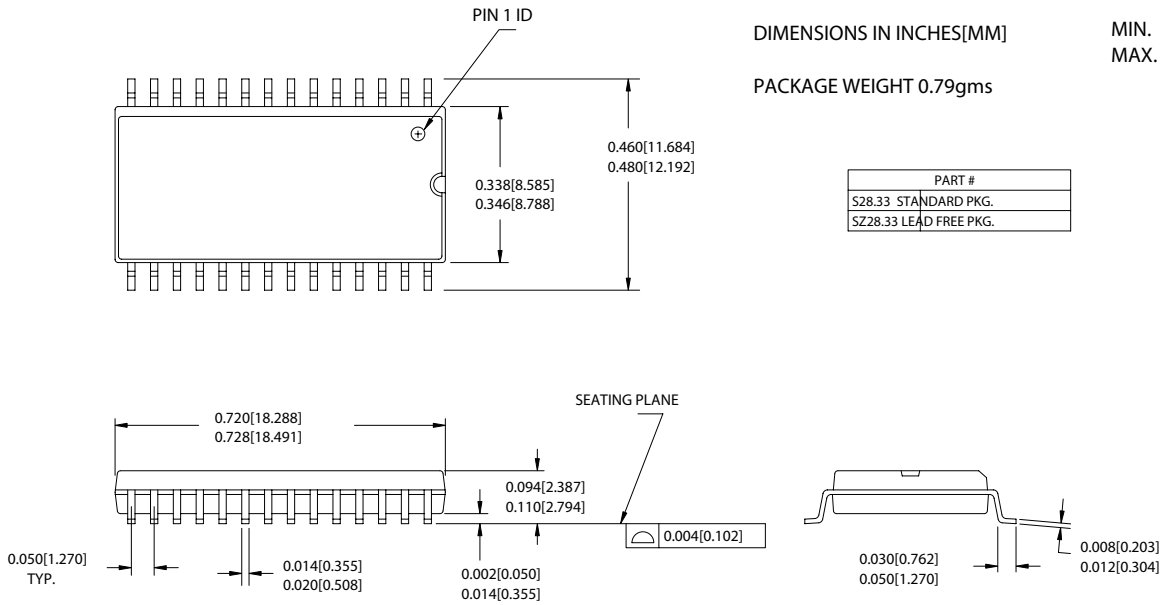
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY6264-55SC	S28.33	28-Lead 330-Mil SOIC <sup>[13]</sup>	Commercial
70	CY6264-70SC	S28.33	28-Lead 330-Mil SOIC <sup>[13]</sup>	Commercial
55	CY6264-55SNC	SN28	28-Lead 300-Mil SOIC	Commercial
55	CY6264-55SNXC	SN28	28-Lead 300-Mil SOIC (Pb-free)	Commercial
70	CY6264-70SNC	SN28	28-Lead 300-Mil SOIC	Commercial
70	CY6264-70SNXC	SN28	28-Lead 300-Mil SOIC (Pb-free)	Commercial
70	CY6264-70SNI	SN28	28-Lead 300-Mil SOIC	Industrial
70	CY6264-70SNXI	SN28	28-Lead 300-Mil SOIC (Pb-free)	Industrial

Shaded areas contain advance information.

**Package Diagrams**
**28-lead (300 mil) SNC Package Outline (Narrow Body) SN28**


51-85092-\*B



**Package Diagrams (continued)**
**28-Lead SOIC with Wide Body S28.33**


51-85058-B

**Document History Page**

<b>Document Title: CY6264 8K x 8 Static RAM</b> <b>Document Number: 001-02367</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	384870	See ECN	PCI	Spec # change from 38-00425 to 001-02367