User's Guide
SLVUAA9B–August 2014–Revised February 2020

Powering the AM335x, AM437x, and AM438x with TPS65218D0

This user's guide is a reference for connectivity between the TPS65218D0 power management IC (PMIC) and the AM335x, AM437x, or AM438x processor. For detailed information about the TPS65218D0, AM335x, AM437x, or AM438x, see their respective data sheets.

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Trademarks

1 TPS65218D0 Overview

The TPS65218D0 is an optimized and highly integrated power management solution for the AM335x, AM437x, and AM438x processor. Features of the TPS65218D0 include:

- Three DC-DC step-down converters
- One LDO

- Three load switches
- Two micro-power DC-DC step-down converters
- Power path management for battery backup of the processor RTC
- Integrated voltage supervisor

2 Connection Diagram for TPS65218D0 and AM335x

The block diagram shown in Figure 1 shows the connections between the TPS65218D0 and the AM335x. Power rails and digital and analog signals are shown. The power rails may be used to power additional parts of the system.

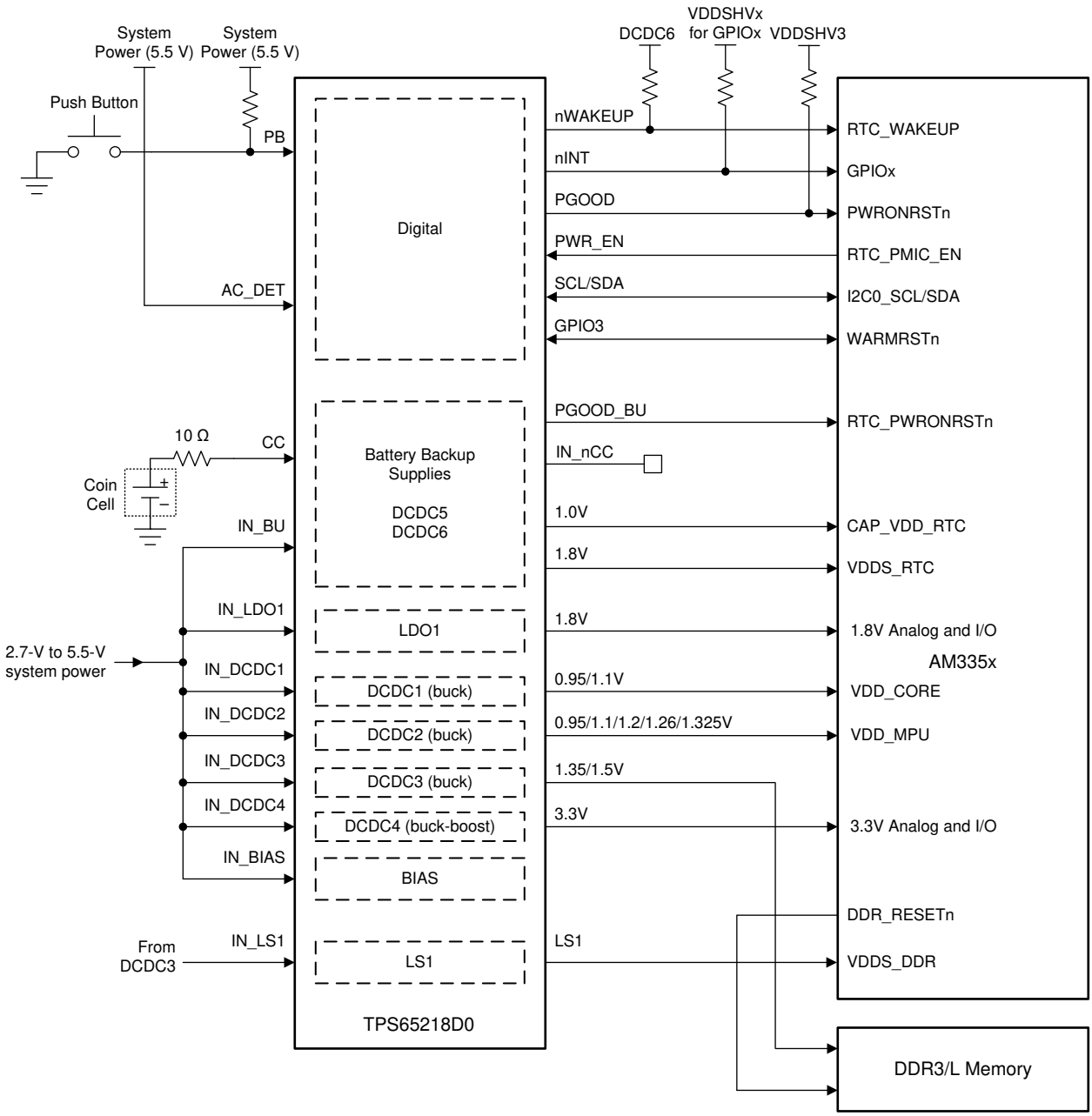

Figure 1. Connection Diagram for TPS65218D0 and AM335x

3 Power Rails for TPS65218D0 and AM335x

Table 1 matches the AM335x power terminals with the appropriate power rail from the TPS65218D0.

Table 1. Power Rails for TPS65218D0 and AM335x

TPS65218D0	Voltage (V)	AM335x
DCDC1	0.95/1.1	VDD_CORE
DCDC2	0.95/1.1/1.2/1.26/1.325	VDD_MPU
DCDC3	1.35/1.5	DDR3L/DDR3 Memory VDDS_DDR
DCDC4	3.3	VDDSHVx (3.3 V)
		VDDA3P3V_USB0/1
DCDC5	1.0	CAP_VDD_RTC
DCDC6	1.8	VDDS_RTC
LDO1	1.8	VDDS
		VDDSHVx (1.8 V)
		VDDS_SRAM_CORE_BG
		VDDS_SRAM_MPU_BB
		VDDS_PLL_DDR
		VDDS_PLL_CORE_LCD
		VDDS_OSC
		VDDA1P8V_USB0/1
		VDDA_ADC

DCDC3 voltage is initially selected through the choice of resistor on the DC34_SEL pin. Each output voltage can be changed dynamically while the TPS65218D0 is in active mode. This requires the use of I^2C commands to the TPS65218D0.

4 Connection Diagram for TPS65218D0 and AM437x

The block diagram shown in Figure 2 shows the connections between the TPS65218D0 and AM437x. Power rails and digital and analog signals are shown. The power rails may be used to power additional parts of the system.

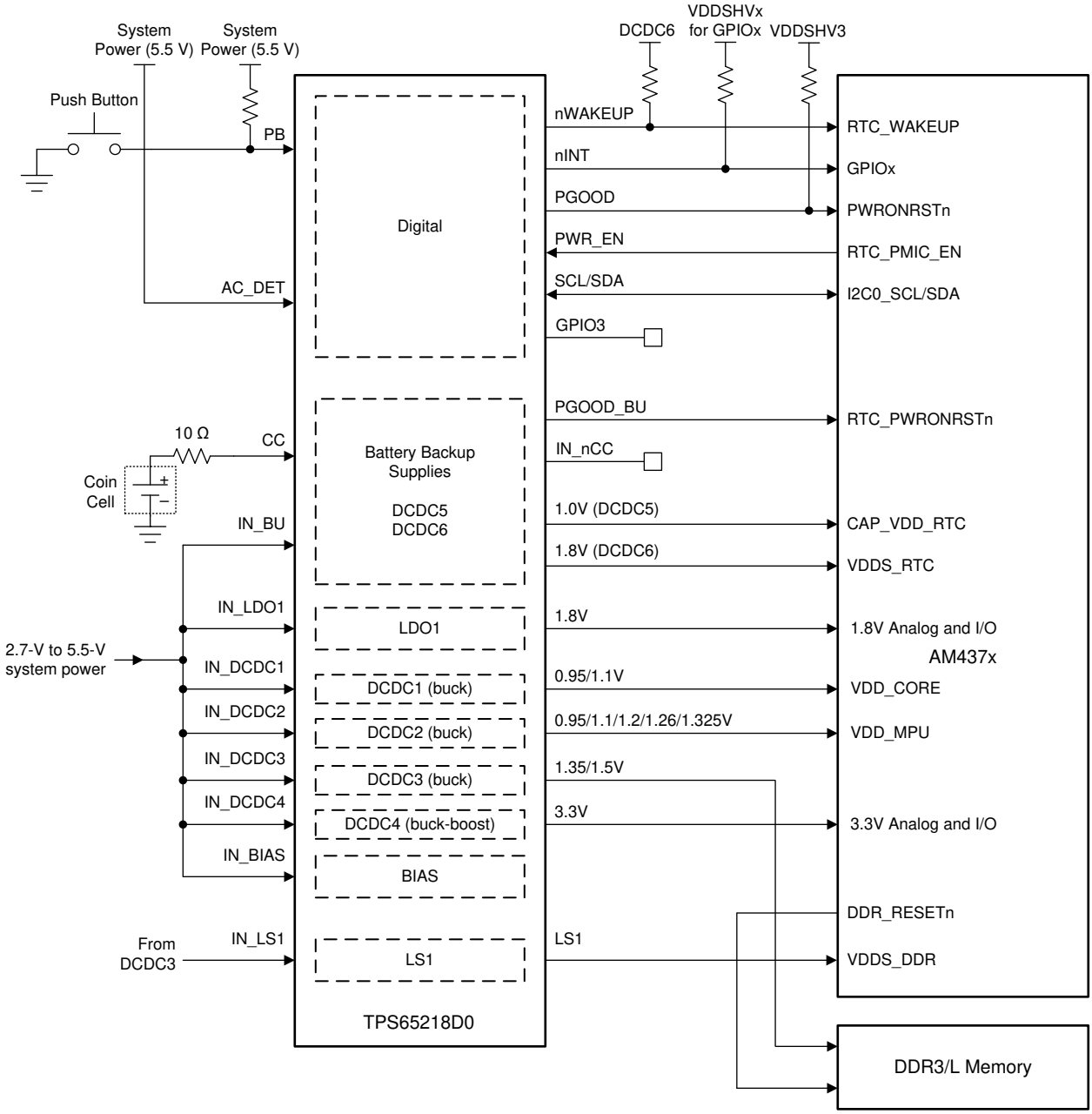

Figure 2. Connection Diagram for TPS65218D0 and AM437x

5 Power Rails Connections for TPS65218D0 and AM437x

Table 2 matches the AM437x power terminals with the appropriate power rail from the TPS65218D0.

Table 2. Power Rails for TPS65218D0 and AM437x

TPS65218D0	Voltage (V)	AM437x
DCDC1	0.95/1.1	VDD_CORE
DCDC2	0.95/1.1/1.2/1.26/1.325	VDD_MPU
DCDC3	1.2/1.35/1.5	LPDDR2/DDR3L/DDR3 Memory
DCDC4	3.3	VDDSHVx(3.3 V)
		VDDA3P3V_USB0/1
		VDDS3P3V_IOLDO
DCDC5	1.0	CAP_VDD_RTC
DCDC6	1.8	VDDS_RTC
LDO1	1.8	VDDS
		VDDSHVx(1.8 V)
		VDDS_SRAM_CORE_BG
		VDDS_SRAM_MPU_BB
		VDDS_PLL_DDR
		VDDS_PLL_CORE_LCD
		VDDS_OSC
		VDDA1P8V_USB0/1
		VDDA_ADC0/1
		VDDS_PLL_MPU
		VDDS_CLKOUT
LS1	1.2/1.35/1.5 (Tied to DCDC3)	VDDS_DDR

DCDC3 voltage is initially selected through the choice of resistor on the DC34_SEL pin. Each output voltage can be changed dynamically while the TPS65218D0 is in active mode. This requires use of I^2C commands to the TPS65218D0.

6 Connection Diagram for TPS65218D0 and AM438x

The block diagram shown in Figure 3 shows the connections between the TPS65218D0 and AM438x. Power rails and digital and analog signals are shown. The power rails may be used to power additional parts of the system.

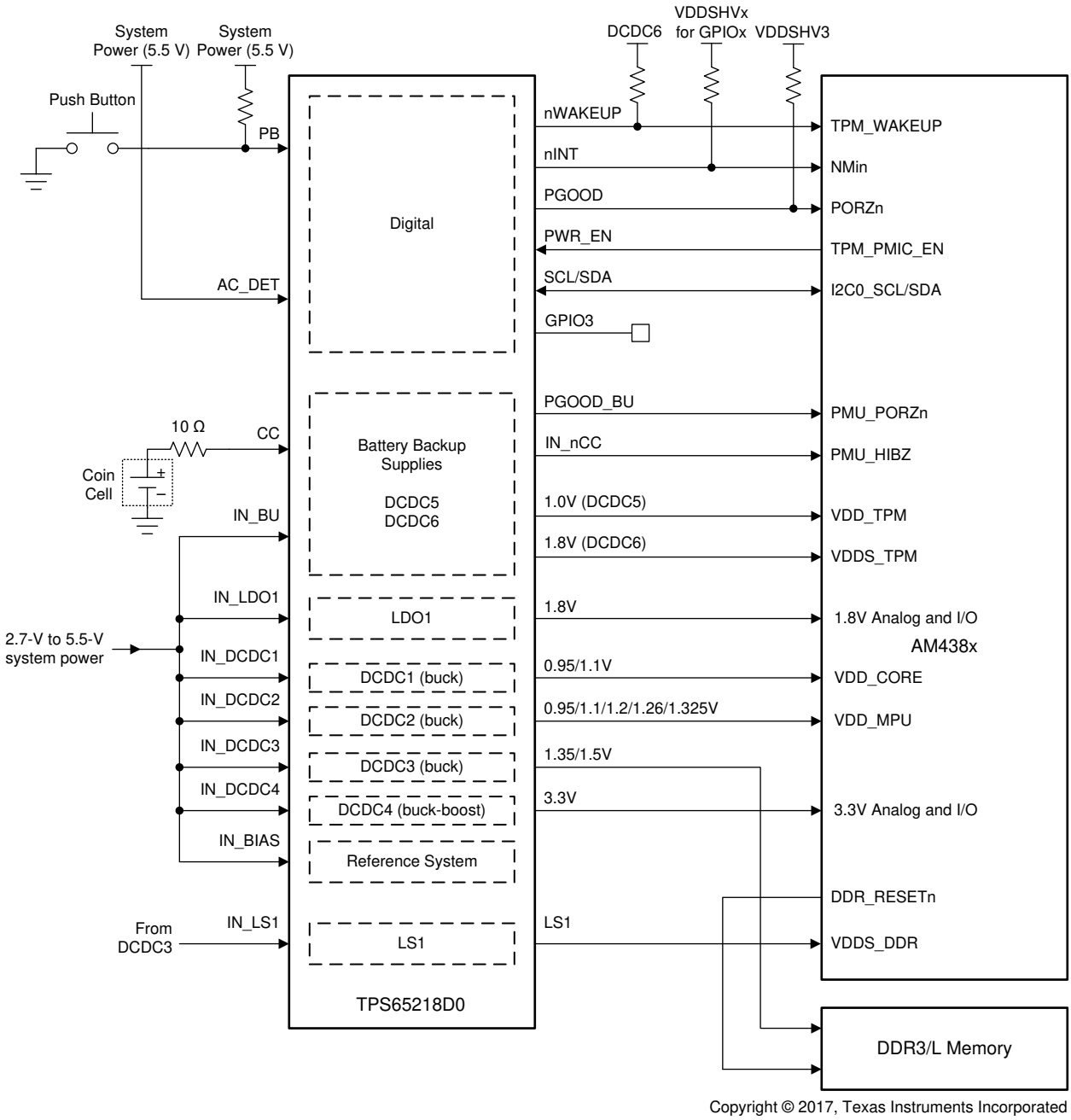

Figure 3. Connection Diagram for TPS65218D0 and AM438x

7 Power Rails Connections for TPS65218D0 and AM438x

Table 3 matches the AM438x power terminals with the appropriate power rail from the TPS65218D0.

Table 3. Power Rails for TPS65218D0 and AM438x

TPS65218D0D0	Voltage (V)	AM438x
DCDC1	0.95/1.1	VDD_CORE
DCDC2	0.95/1.1/1.2/1.26/1.325	VDD_MPU
DCDC3	1.2/1.35/1.5	LPDDR2/DDR3L/DDR3 Memory
DCDC4	3.3	VDDSHVx(3.3 V)
		VDDA3P3V_USB0/1
		VDDS3P3V_IOLDO
DCDC5	1.0	VDD_TPM
DCDC6	1.8	VDDS_TPM
LDO1	1.8	VDDS
		VDDSHVx(1.8 V)
		VDDS_SRAM_CORE_BG
		VDDS_SRAM_MPU_BB
		VDDS_PLL_DDR
		VDDS_PLL_CORE_LCD
		VDDS_OSC
		VDDA_1P8V_USB0/1
		VDDA_ADC0/1
		VDDS_PLL_MPU
		VDDS_CLKOUT
LS1	1.2/1.35/1.5 (Tied to DCDC3)	VDDS_DDR

DCDC3 voltage is initially selected through the choice of resistor on the DC34_SEL pin. Each output voltage can be changed dynamically while the TPS65218D0 is in active mode. This requires use of I^2C commands to the TPS65218D0.

NOTE: The TPS65218D0 device should be used for AM438x processor.

8 Power-Up and Power-Down Sequence for TPS65218D0

Figure 4 describes the power-up and power-down sequence of the TPS65218D0. This sequence is specifically optimized for the AM335x, AM437x, and AM438x processor.

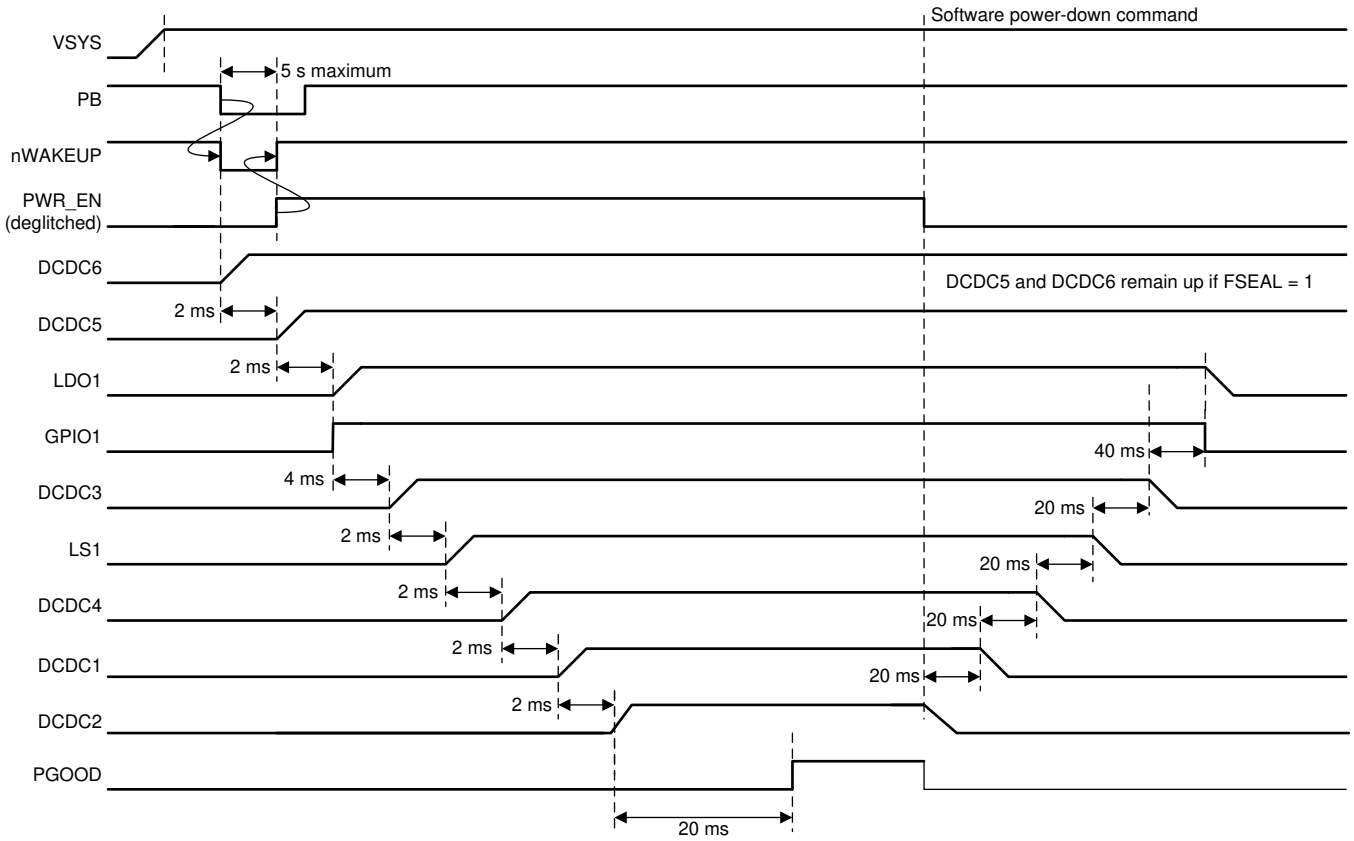

Figure 4. TPS65218D0 Sequence Timing Diagram

The power-up sequence is defined by a series of ten strobes and nine delay times. Each output rail is assigned to a strobe to determine the order in which the rails are enabled. The delay time in-between strobes is 2 ms by default. Table 4 lists the default strobe assignments for TPS65218D0.

Table 4. TPS65218D0 Power-Up Sequence

Strobe 1	DCDC6
Strobe 2	DCDC5
Strobe 3	LDO1
	GPIO1
Strobe 4	
Strobe 5	DCDC3
Strobe 6	
Strobe 7	DCDC4
Strobe 8	DCDC1
Strobe 9	DCDC2
Strobe 10	

9 Memory Voltage Selection

DCDC3 can be configured to support a variety of DDR memory voltages. The desired voltage can be selected by placing a 1% resistor to ground on the DC34_SEL pin. Table 5 lists the available memory voltages and the needed resistor for each.

Table 5. DCDC3 Voltage Selection

Memory	DCDC3 Voltage (V)	Resistor (kΩ)
LPDDR2	1.2	0 (tie to ground)
DDR3L	1.35	12.1
DDR3	1.5	20
DDR2	1.8	31.6

10 Using LPDDR2 Memory

If LPDDR2 memory is used, an additional 1.8 V LDO is required. GPIO1 is programmed to properly sequence the additional LDO and should be tied to the LDO enable pin as seen in Figure 5.

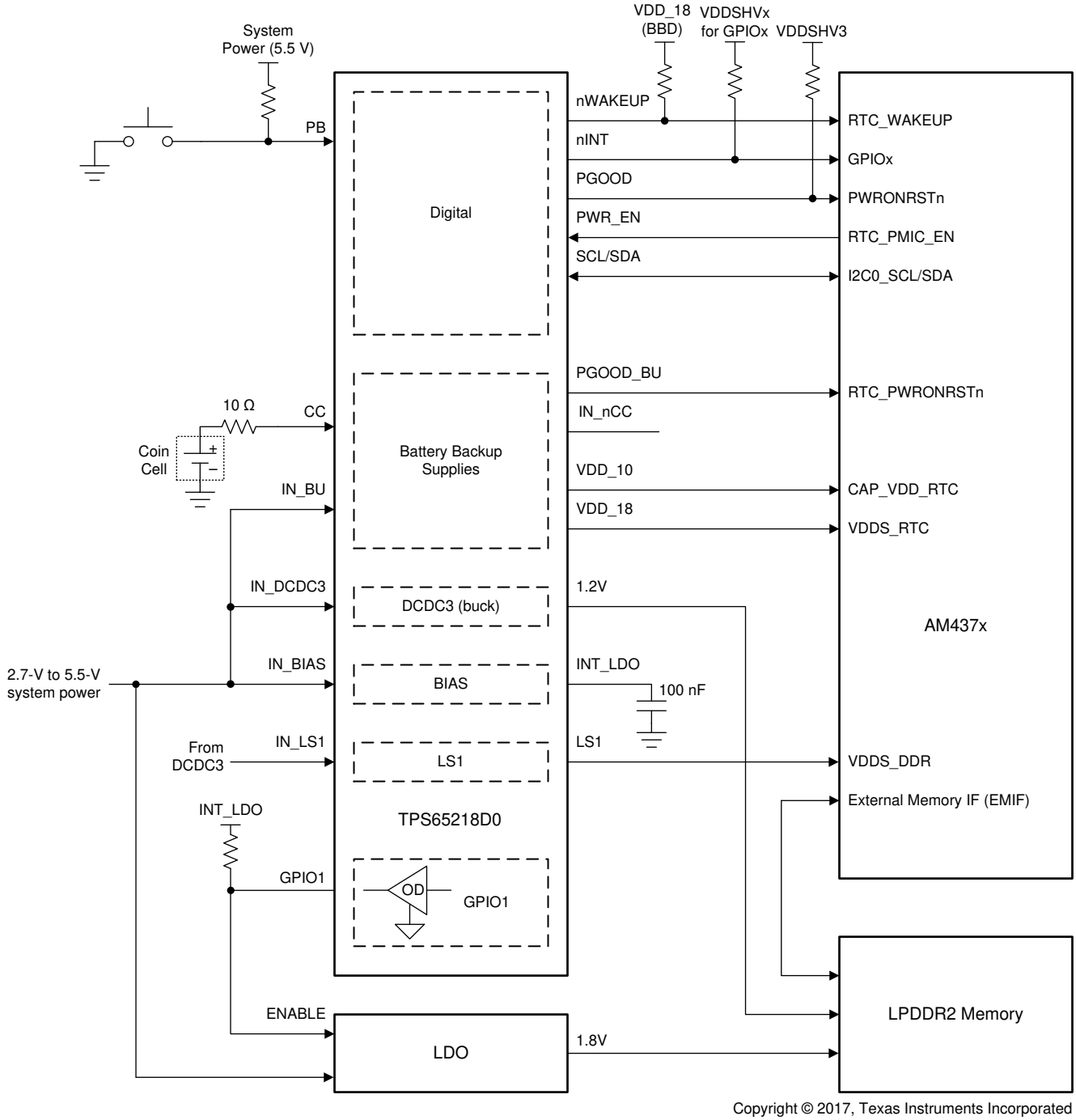

Figure 5. Connection Diagram for TPS65218D0, AM437x, and LPDDR2 Memory

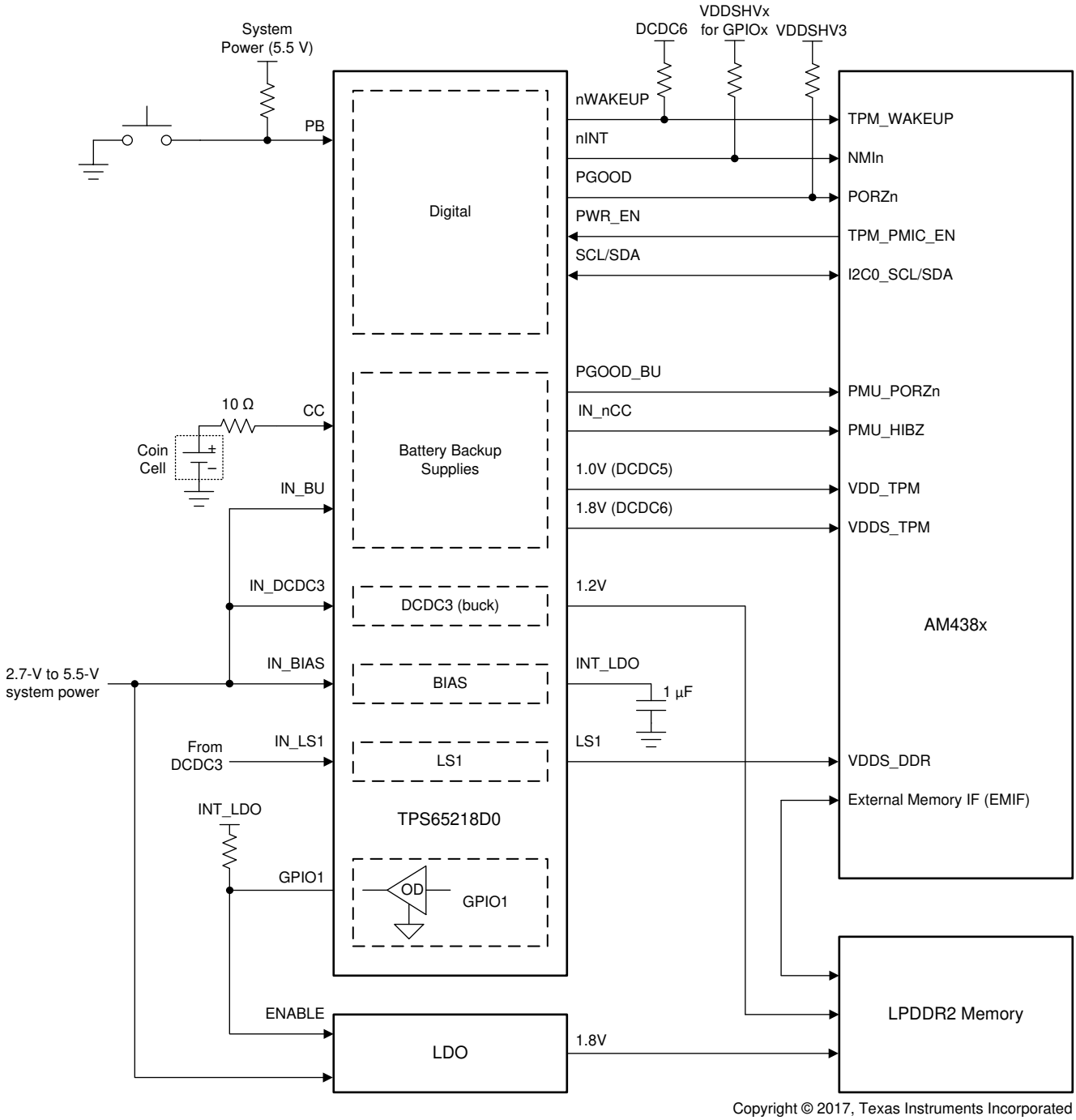

Figure 6. Connection Diagram for TPS65218D0, AM438x, and LPDDR2 Memory

11 Warm Reset

The TPS65218D0 supports warm reset functionality with the AM335x processor. This functionality is enabled on the TPS65218D0 by default, and can be disabled through I^2C. When enabled, GPIO3 acts as the warm reset input to the PMIC. Asserting GPIO3 low causes DCDC1 and DCDC2 to slew back to their default value of 1.1 V.

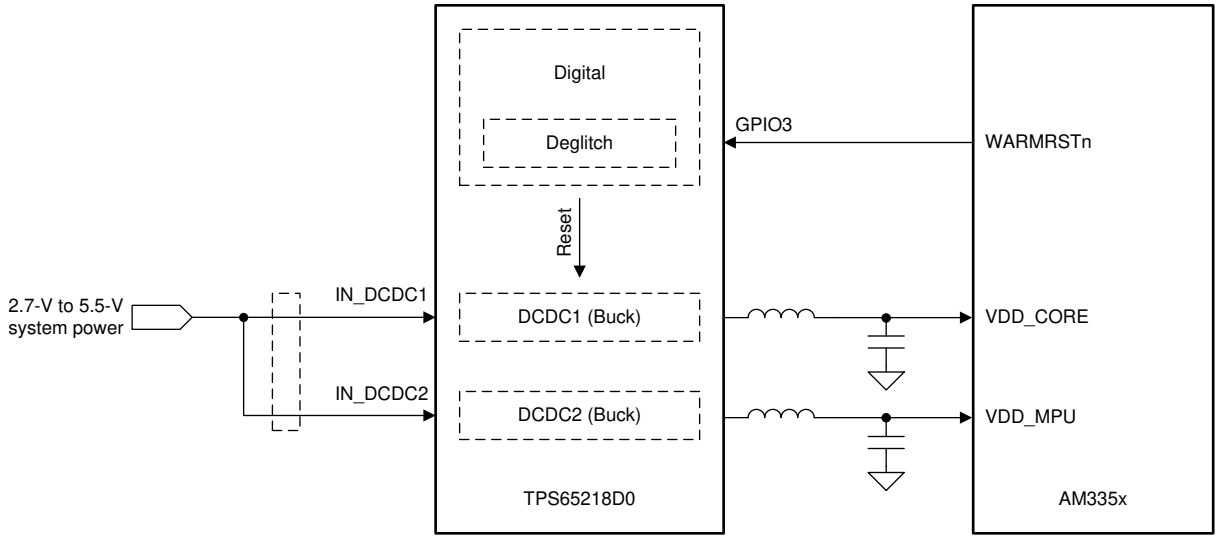

Figure 7. Warm Reset Functionality

12 Pullup Resistors

There are several pullup resistors needed for operating the TPS65218D0 with the AM335x, AM437x, or AM438x processor. PB should be pulled up to VSYS. nWakeup should be pulled to DCDC6 so that the pullup source is present even during SUSPEND and OFF mode. A 100-kΩ pullup resistor should be used for nWakeup to minimize the current load on DCDC6. nINT, PGOOD, SCL, and SDA should be pulled up to the same supply that powers VDDSHVx for each signal. SCL and SDA use lower value pullups resistors in order to decrease rise time of these nodes during I^2C communication.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2014) to A Revision	Page
• Added the *TPS65218D0D0* and *AM438x* Connection Diagram	6

Changes from A Revision (August 2017) to B Revision	Page
• Changed device From: *TPS65218* To: *TPS65218D0*	1

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