Revision History

PCN #	Issue Date	Description
02A-22	September 26, 2022	Initial Release

Subject: PCN#02-22 Notification of Changes to CrossLink-NX™, Certus-NX™ and CertusPRO-NX™ Data Sheets

Dear Lattice Customer,

Lattice Semiconductor is providing this notification of changes to the CrossLink-NX Family Data Sheet (FPGA-DS-02049), Certus-NX Family Data Sheet (FPGA-DS-02078) and CertusPro-NX Family Data Sheet (FPGA-DS-02086).

These changes will be included in the new CrossLink-NX Family Data Sheet (FPGA-DS-02049 version 1.5 dated September 2022) , Certus-NX Family Data Sheet (FPGA-DS-02078 version 1.3 dated September 2022) and CertusPro-NX Family Data Sheet (FPGA-DS-02086, version 1.2 dated September 2022). The changes are described below.

Change Description

The following primary changes have been made to the datasheets:

1) Increases the minimum PLL Input Clock Frequency

2) Clarifies the Phase Jitter specification of the PLL.

3)The following changes have been made with respect to SGMII support:

- Removed SGMII support specifically for CrossLink-NX devices in the 72-ball WLCSP and 72-pin QFN
- Extended SGMII support to automotive grade products for CrossLink-NX, Certus-NX and CertusPRO-NX

4) Added additional detail regarding I/O Overshoot and Undershoot specifications

5) Please review the Data Sheet Revision History for additional corrections and minor updates.

Detailed Explanation

(1) Increase in Minimum PLL Input Clock Frequency

The PLL Input Clock Frequency, f_{IN} (sometime referred to as the Reference Clock Frequency) mimimum value is increased from 10 MHz to 18 MHz. Correspondingly, the Phase Detector Input Frequency (f_{PFD}) minimum, with and without Fractional-N synthesis, f_{PFD}, is increased from 10 MHz to 18 MHz.

(2) Clarify the Phase Jitter specification

The PLL Output Clock Phase Jitter portion of t_{OPJIT} specification is updated to eliminate ambiguity and more closely reflect expected PLL performance. For f_{PFD} values below 200 MHz, the former specification in UIPP is replaced with absolute ps p-p values in a piecewise linear fashion. This allows designers to more accurately and confidently determine timing and jitter budget margins.

Specific datasheet sections have been updated to reflect this change. The datasheet section to reference is “sysCLOCK PLL Timing” contained in datasheet Section 3 (for Commercial/Industrial grades) and Section 4 (for Automotive grade).

The complete list of affected tables are as follows:

- CrossLink-NX Family Data Sheet (FPGA-DS-02049) Table 3.34 and Table 4.34
- Certus-NX Family Data Sheet (FPGA-DS-02078) Table 3.34 and Table 4.30
- CertusPro-NX Family Data Sheet (FPGA-DS-02086) Table 3.33 and Table 4.33

Please note that the silicon has not been updated and the silicon performance has not changed from any previous material shipments. Lattice is only updating the datasheet performance numbers to match the silicon characteristics.

Effects to Customer Design

Customers are requested to evaluate PLL designs against the updated parameters to determine if there is any impact or exposure. Generally, if an existing design has been fully validated and performs to the customer expection, no action is required.

Customers may use the following criteria to assist their evaluation

Minimum PLL Input Clock Frequency

- Is the PLL Input Clock (Reference Clock) Frequency > 18 MHz?
  - Yes: **No change required**
  - No: Evaluate your design to the updated data sheet parameters.

Phase Jitter specification

- Is the PLL Input Clock Frequency greater than or equal to 100 MHz?
  - Yes. **No change required**
  - No: is this Synthesis Ratio less than or equal to 5 (note 1)?
    - Yes: **No change required**
    - No: Please evaluate your design against the updated specification.

Notes:

1-The Synthesis Ratio is the ratio between the PLL Input Clock Frequency and the highest PLL output frequency.

For example, f_{IN} = 20 MHz, f_{CLKOP}= 100 MHz, f_{CLKOS} = 200 MHz, then the ratio is 200 MHz / 20 MHz = 10

Affected Products

All ordering part numbers for the Crosslink-NX, Certus-NX and CertusPro-NX device families are affected by this PCN.

This PCN also affects all package, grade and tape/reel options and any custom devices (i.e. factory programmed, special test, etc.) which are derived from any of the base devices listed in the family.

Material Set Changes

No changes to Silicon as part of this PCN.

Conversion Timing Summary

The PCN becomes effective immediately upon its release.

Software

Updates to PLL settings within the Lattice Radiant design software are required to meet the new PLL data sheet performance specifications. The software will be updated at the next major software release which will be Lattice Radiant 2022.1 and currently scheduled for late 4Q2022.

Recommended Actions

Customers who have further questions regarding this specification change are encouraged to contact local field support or sales@latticesemi.com.

Lattice PCNs are available on the Lattice website. Please sign up to receive e-mail PCN alerts by registering here. If you already have a Lattice web account and wish to receive PCN alerts, you can do so by logging into your account and making edits to your subscription options.

Sincerely,

Lattice PCN Administrator